



Quicgate NIOSII Reference Design Instructions

Tool version: QUARTUS II 7.2 sp3 / NIOSII IDE 7.2 Build sp3

The following instructions were written using the “quicnios_2C5” design, however, the same instructions can be applied to the “quicnios_2C8” design.

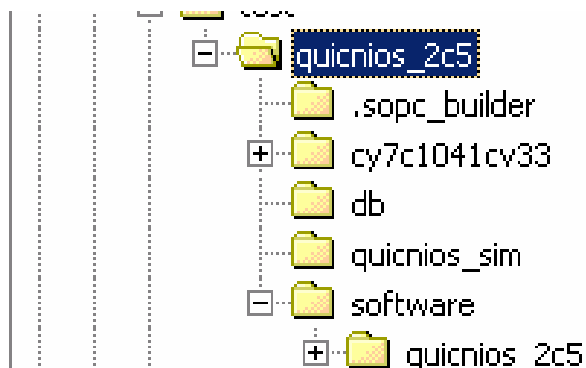
To Begin unzip the quicnios_2cx.zip file in your working directory.

Step 1: Quartus II

The project has been simply zipped instead of archived. This was done because the archive feature does not include custom SOPC components, thus you currently have a complete image of the original build directory. If you choose, you can open the design, open SOPC builder, regenerate the NIOSII core and then recompile the design. This however is not necessary to build and flash the NIOSII software design

Step 2: NIOS II IDE (Importing and system library generation)

- Launch the NIOSII IDE (Take all the defaults unless you are an experience user)

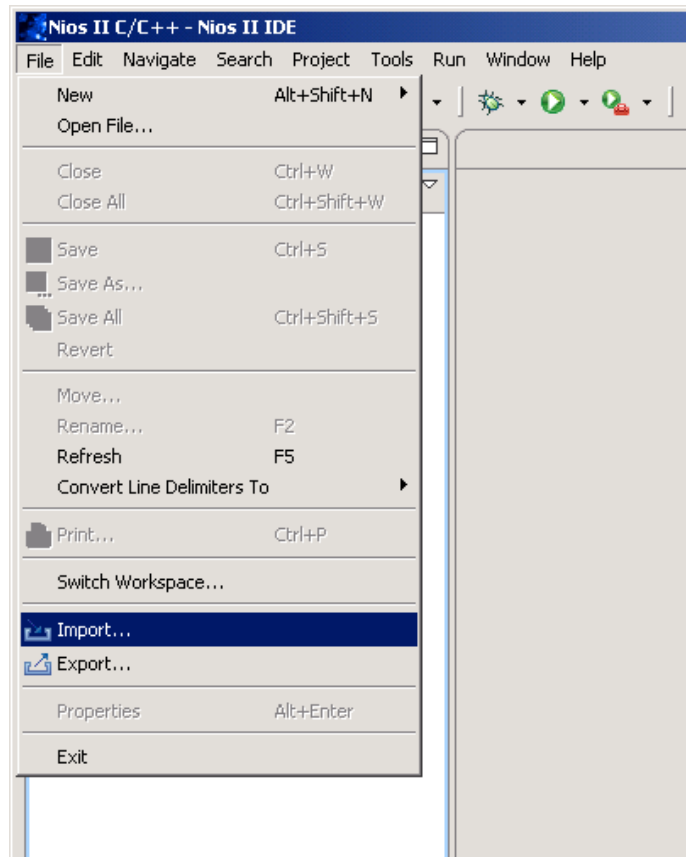


If you look at the unzipped directory you should have a structure similar to the above.

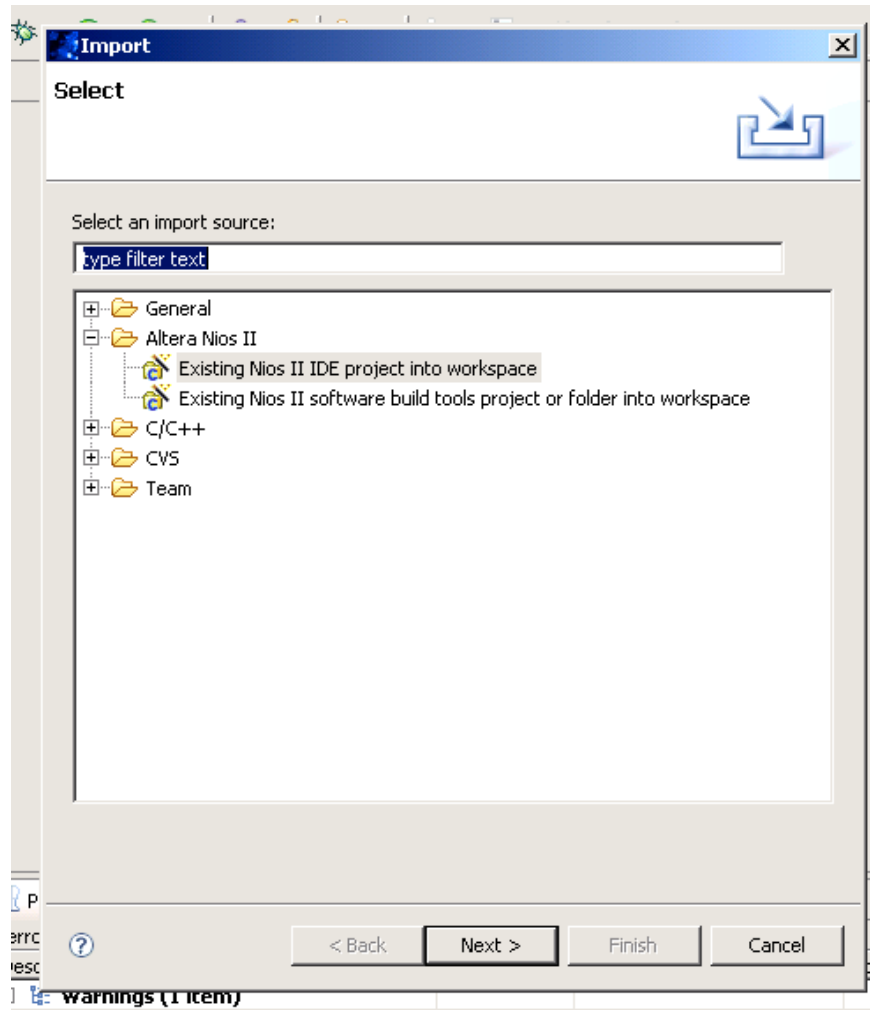
If you have not recompiled the design the “db” directory will be missing. This was done to reduce the size of the zip file and is not required for programming/ flashing.

Notice that under the software directory there is a quicnios_2Cx directory. This is the location of the simple software project. The first step is to import this project into the IDE.

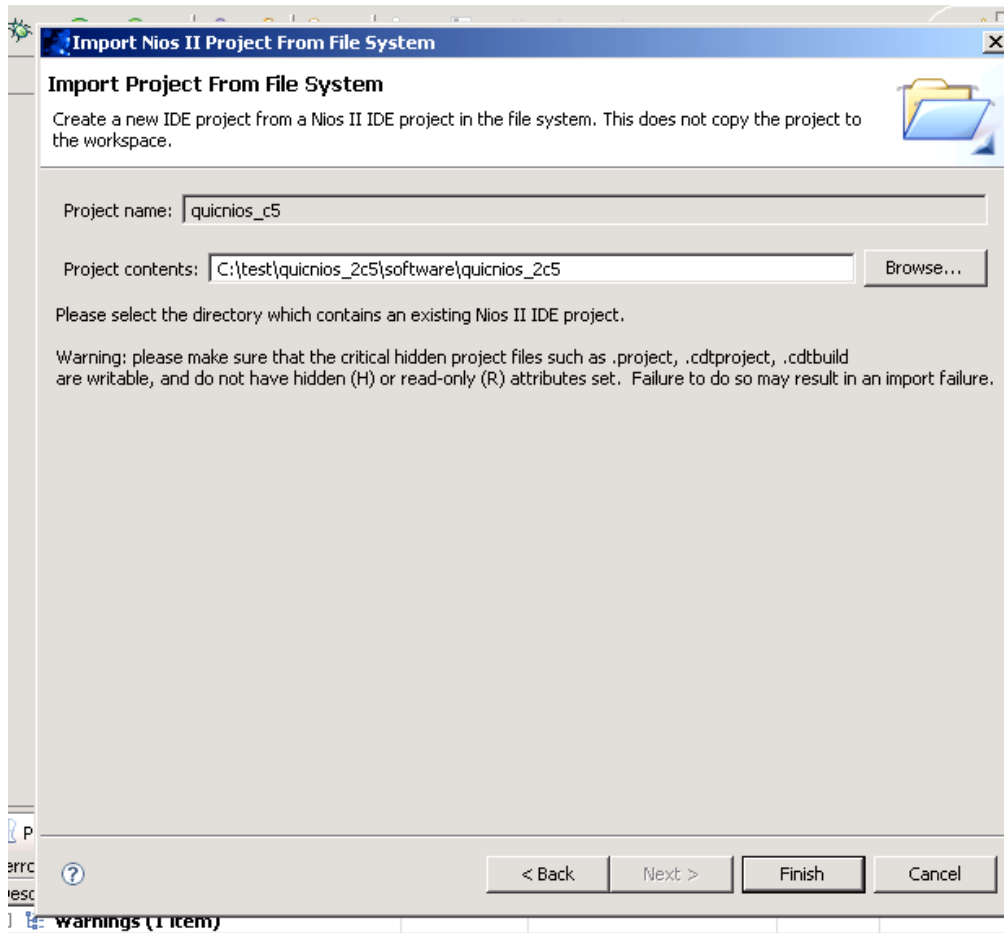
- To import the Quicnios design select “IMPORT” from the file menu. (shown below)



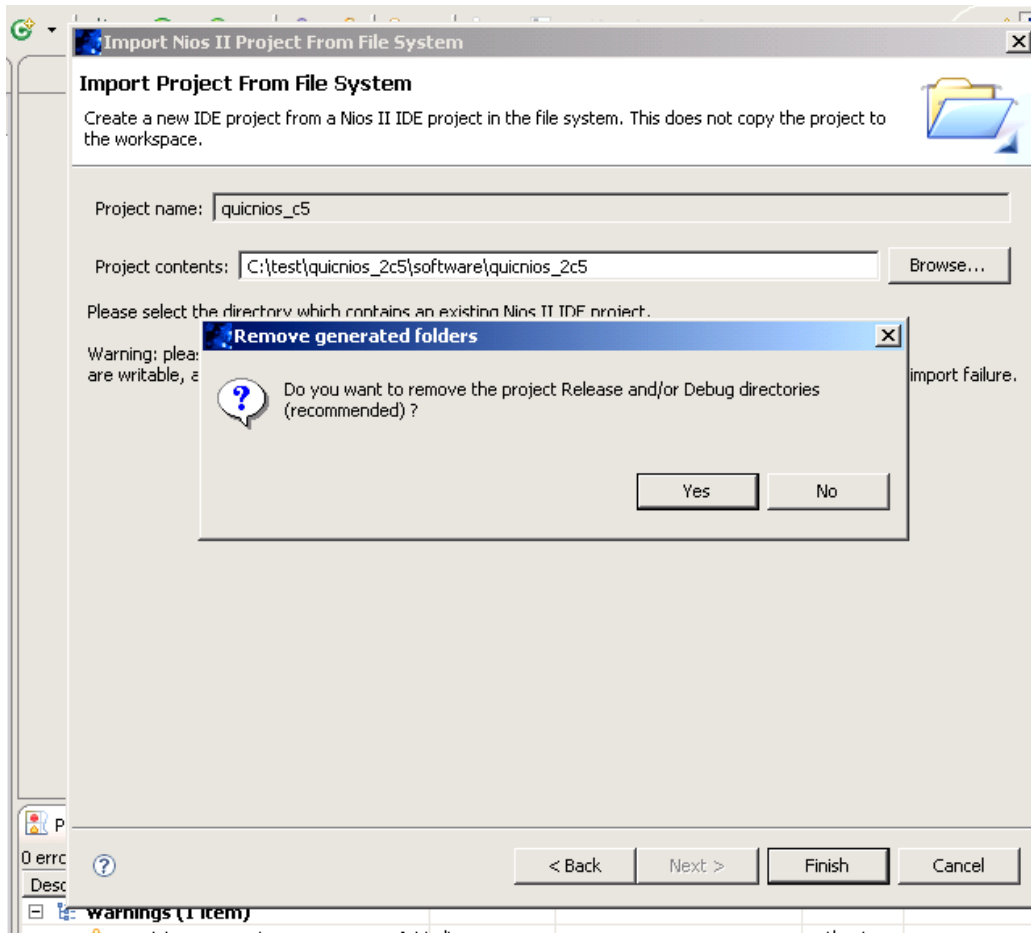
- Once selected the following window will open. (shown below)



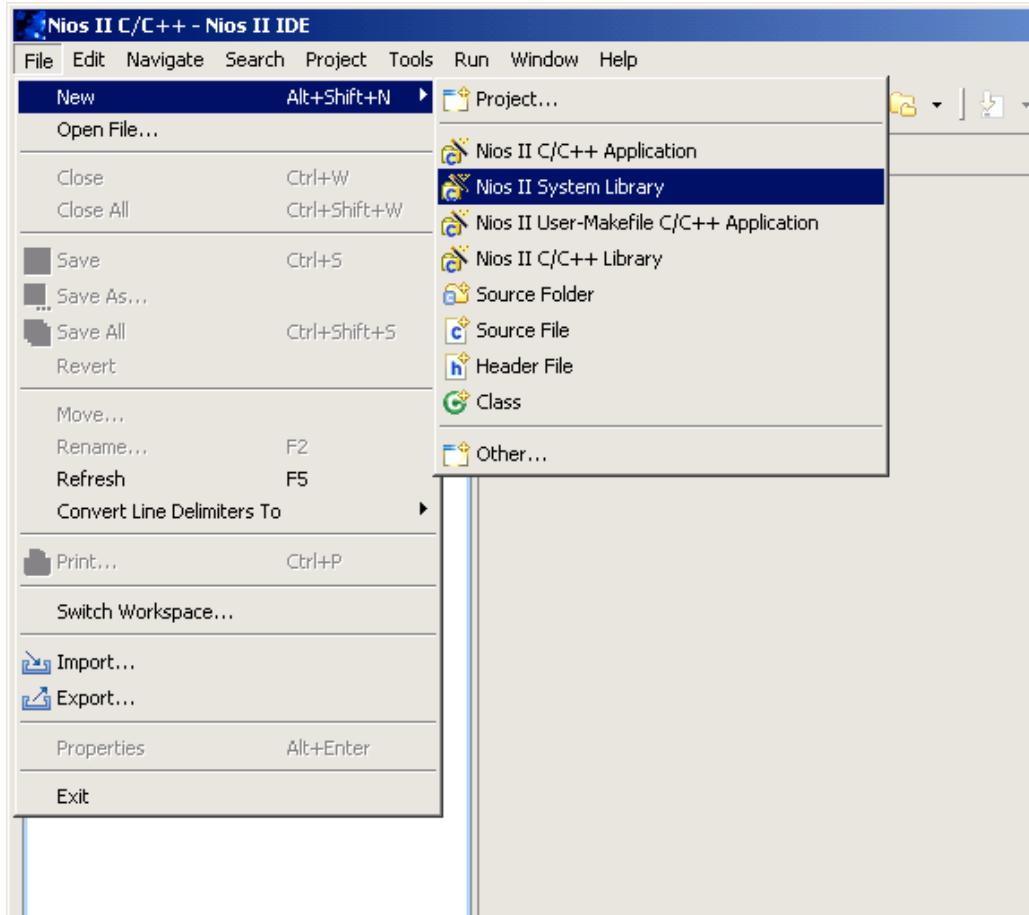
- Select the “Existing Nios II IDE project into workspace” press NEXT



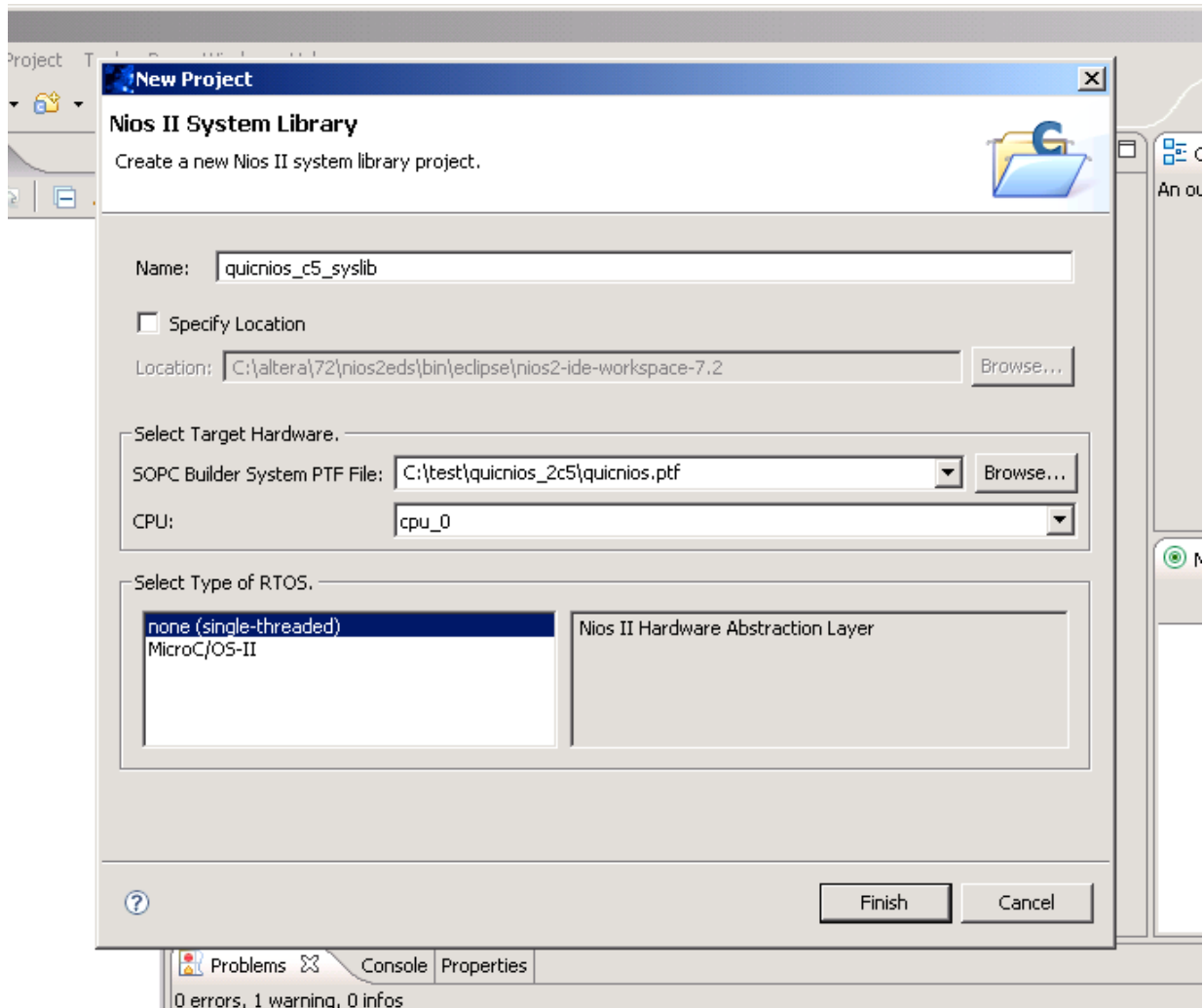
- Browse to the location of the quicnios_2cx design located in the software directory and press FINISH.



- Press Yes to remove the previous RELEASE / DEBUG directories.
- Next, You will need to build a new System library.

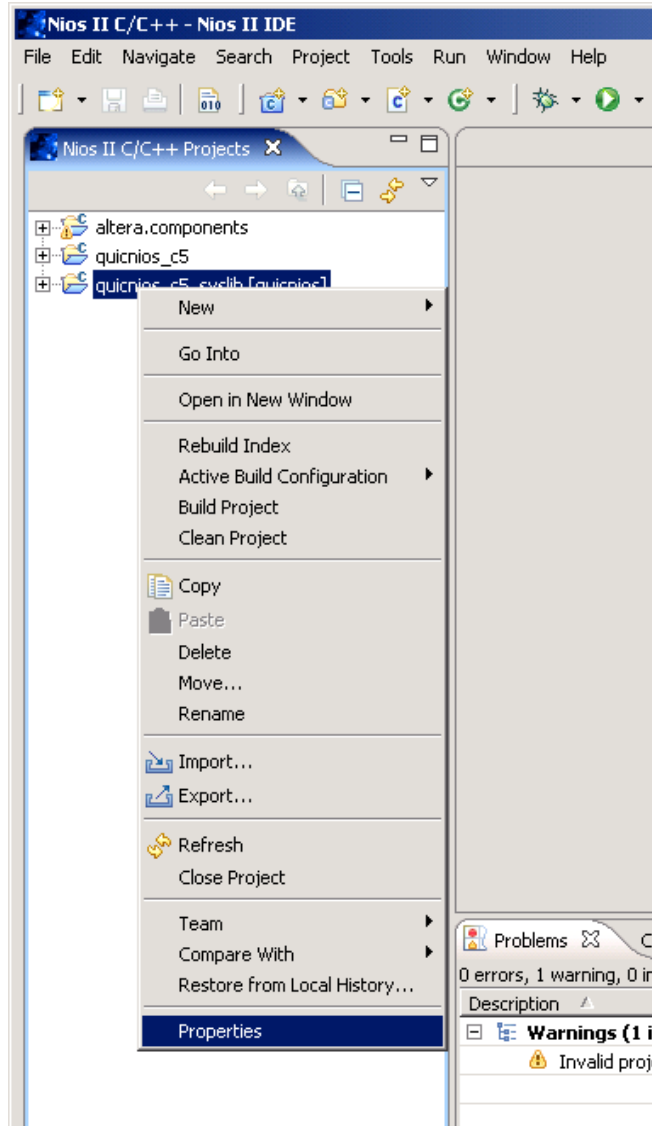


- Under the File pull down tab, select NEW and NIOS II System Library. (Shown above)

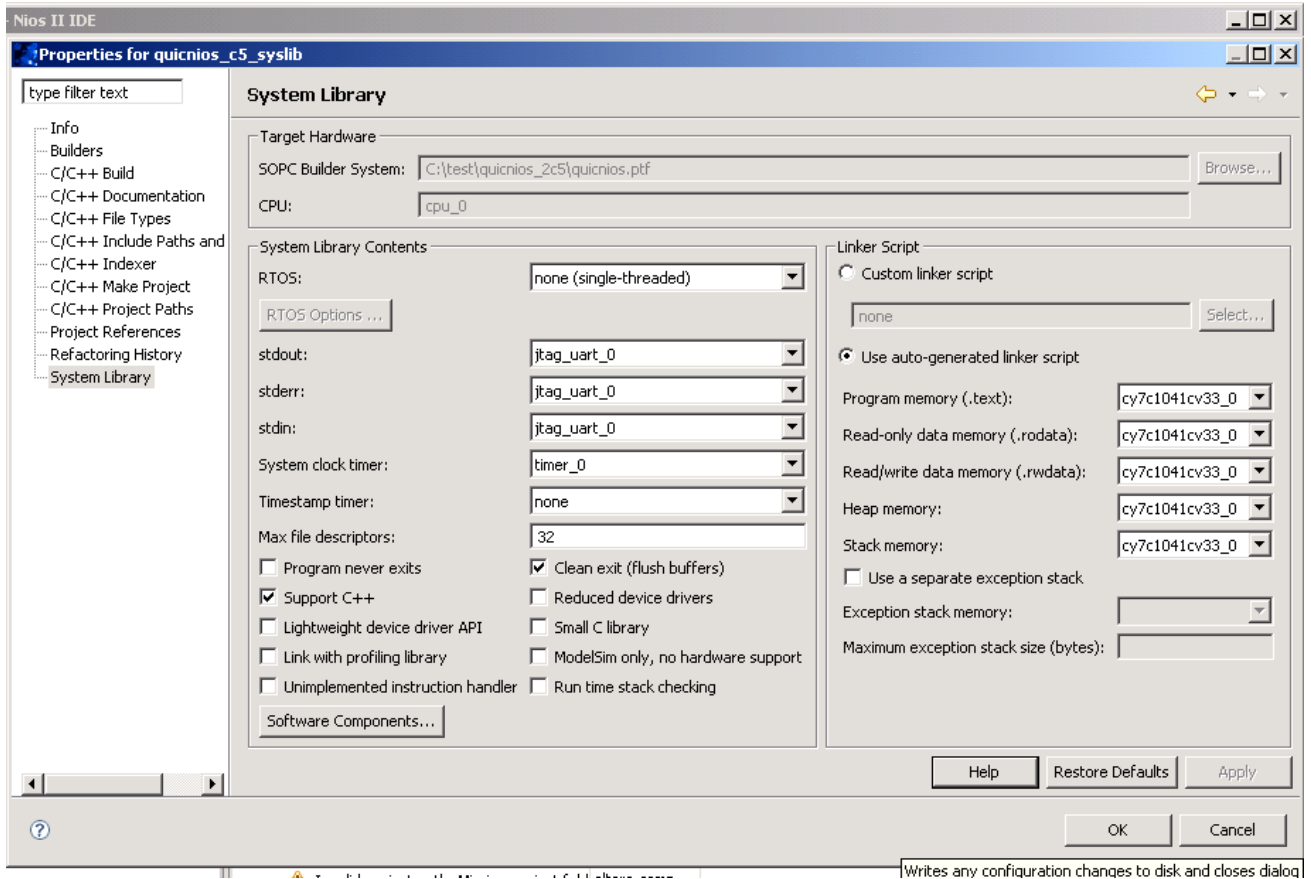


- Setup your system library to look like the above window.

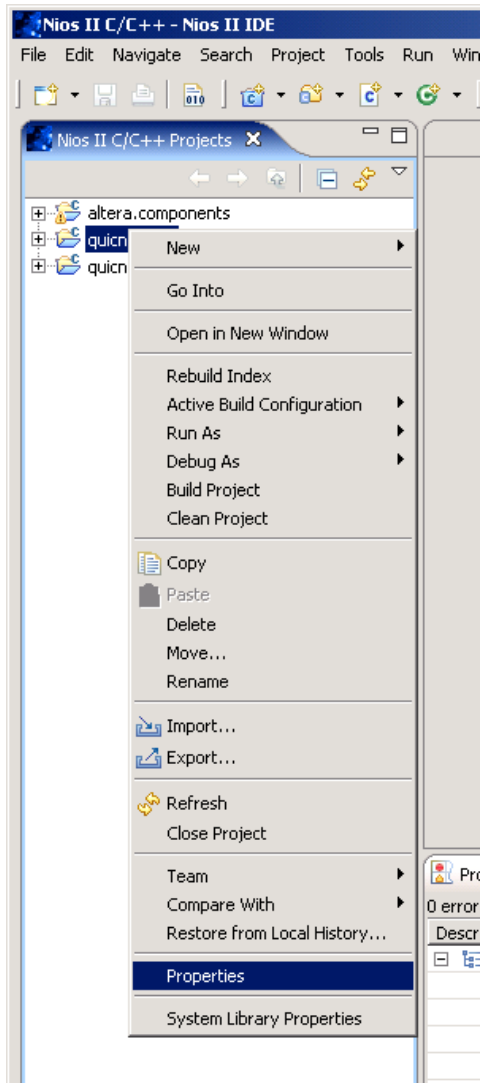
The Name above is quicnios_cx_syslib. Insert either a 5 or 8 for the x depending on the board you are using.



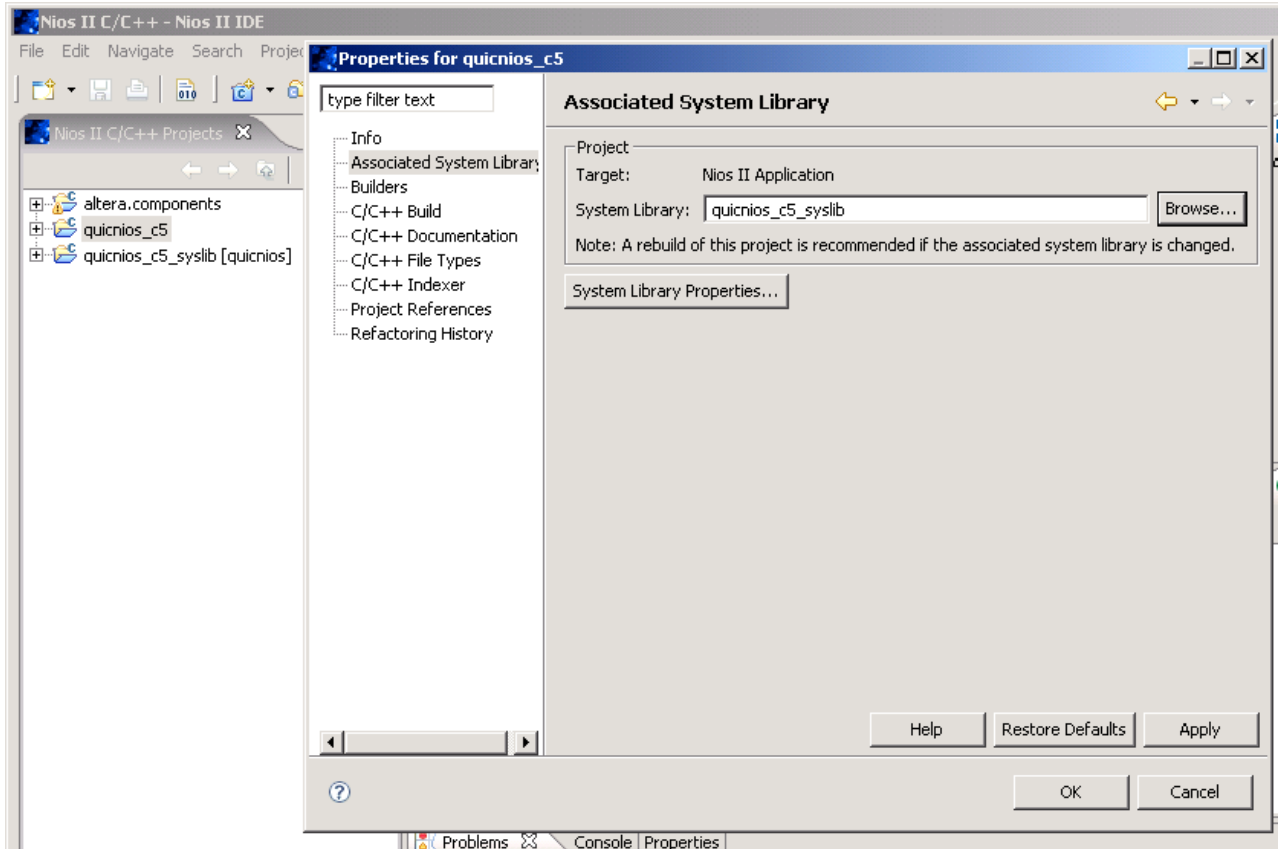
- Next right click over the newly created syslib and select properties.



- Next, setup the syslib panel so that it looks identical to the panel (shown above).

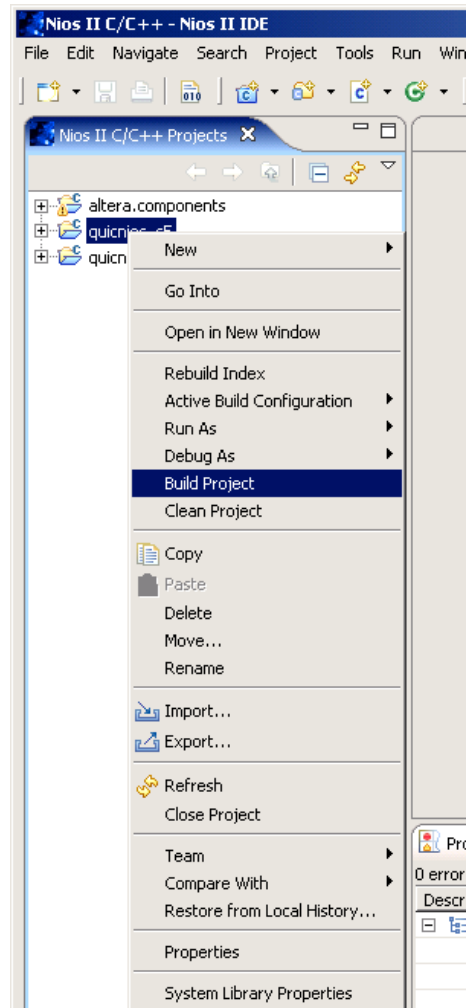


- Right click over the quicnios_2cx directory and select properties (shown above).



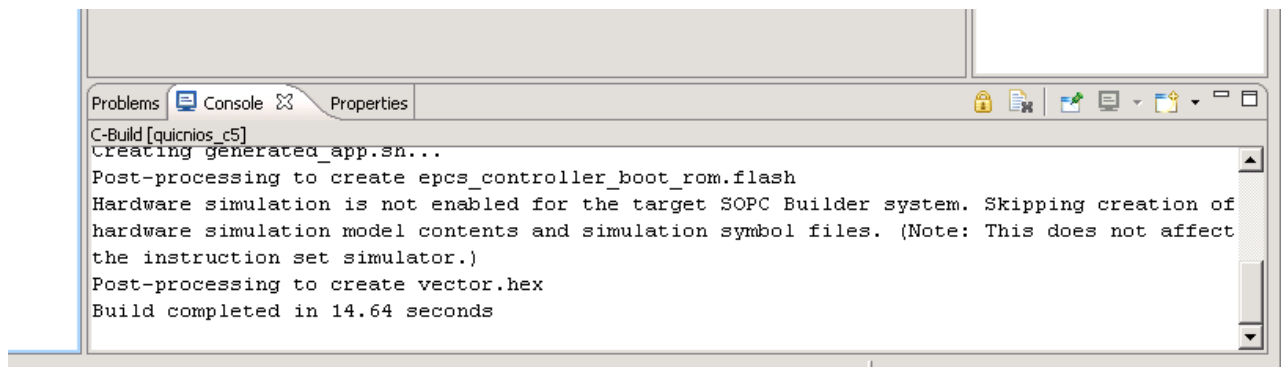
- In the properties for quicnios_2cx window select the “Associated System library” entry and browse to the quicnios_cx_syslib created earlier.

You are now ready to build the project.



- Right click over the quicnios_cx project and select “Build Project”

If the above steps were followed correctly, the build should complete without error (shown below).



Step 3: NIOS II IDE (Quartus II Programmer)

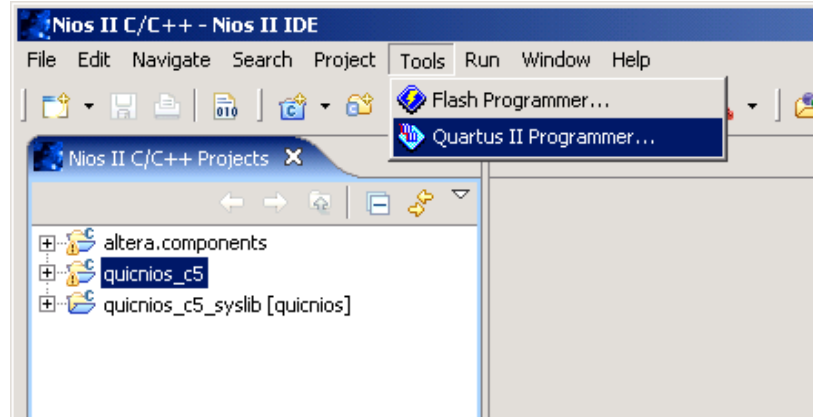
You are now ready to program the quicnios_2cx .sof image into your quicgate board.

This is required in order to Flash the NIOSII software image.

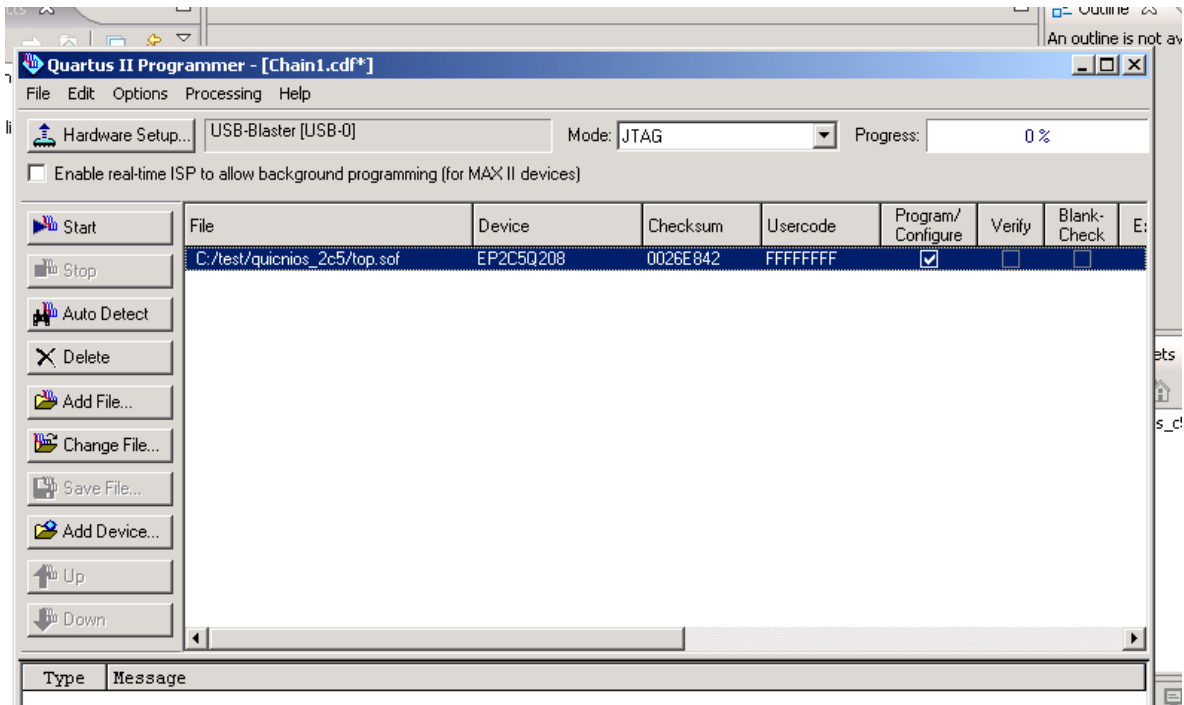
IMPORTANT:

Connect the programmer to the 10 Pin header labeled “JTAG” located on the quicgate module. Be sure that the PIN 1 indicating stripe on the programmer is oriented to the PIN 1 identifier on the quicgate module.

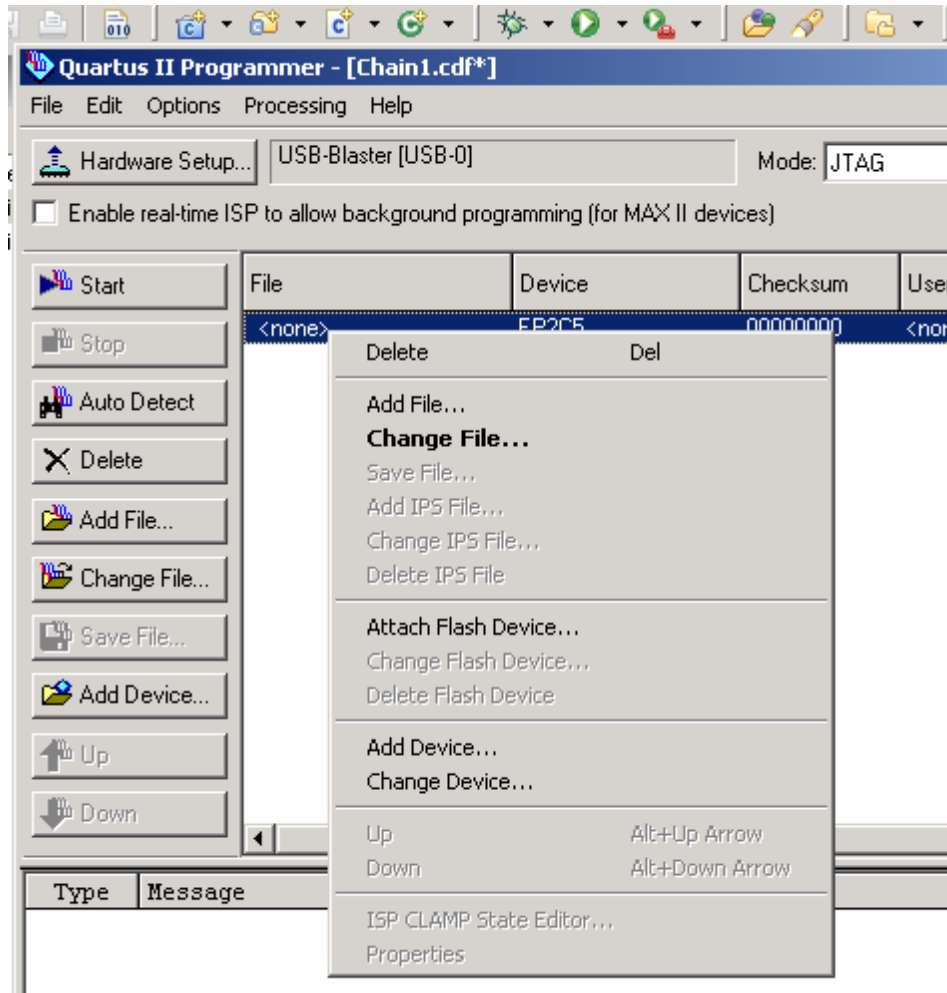
Next apply power to the quicgate module.



- From the “Tools” pull down menu select the Quartus II Programmer. The window below should open.



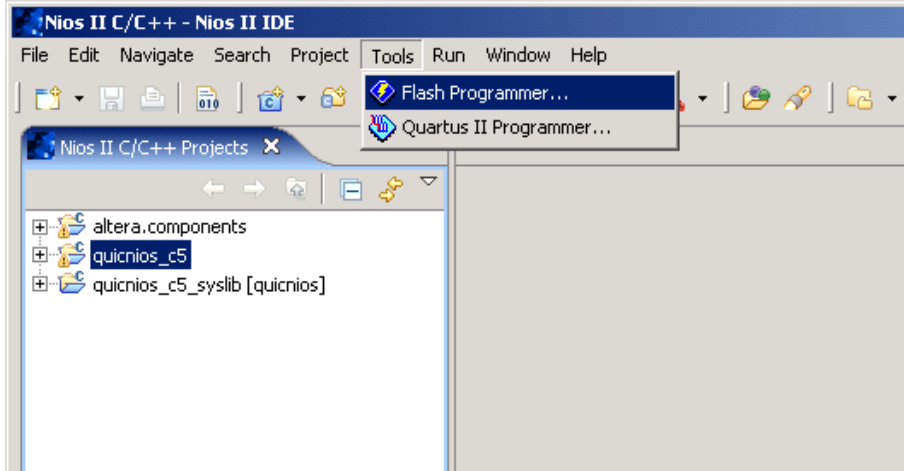
- Press the “Auto Detect” button, the 2cx FPGA should now be an identified device.



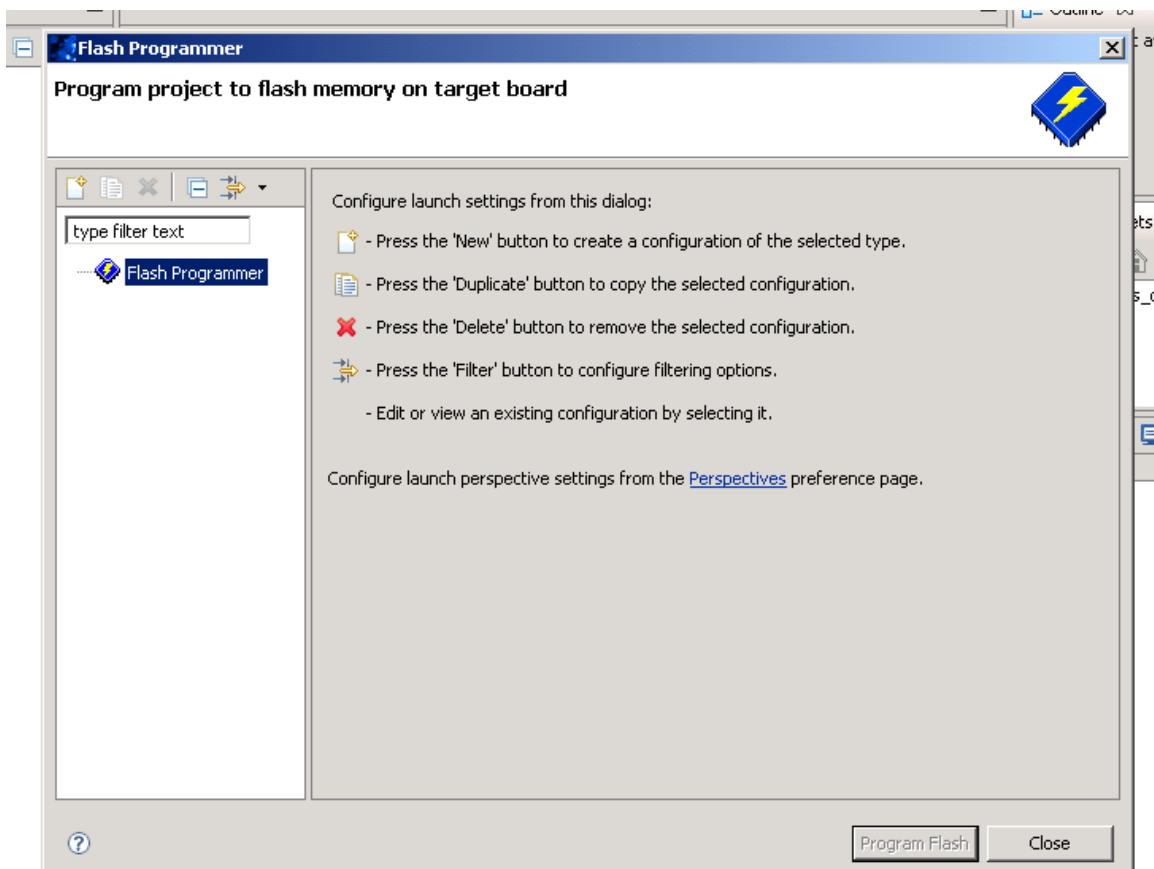
- Right click over the listed device and select “Change File”. Browse to the quicnios_2cx Quartus II project directory and select the “top.sof” file.
- Press the “Start” button. Once the programming operation has completed all of the LEDs on the quicgate module should be ON.
- **Close the programmer.**

Step 3: NIOS II IDE (Flash Programmer)

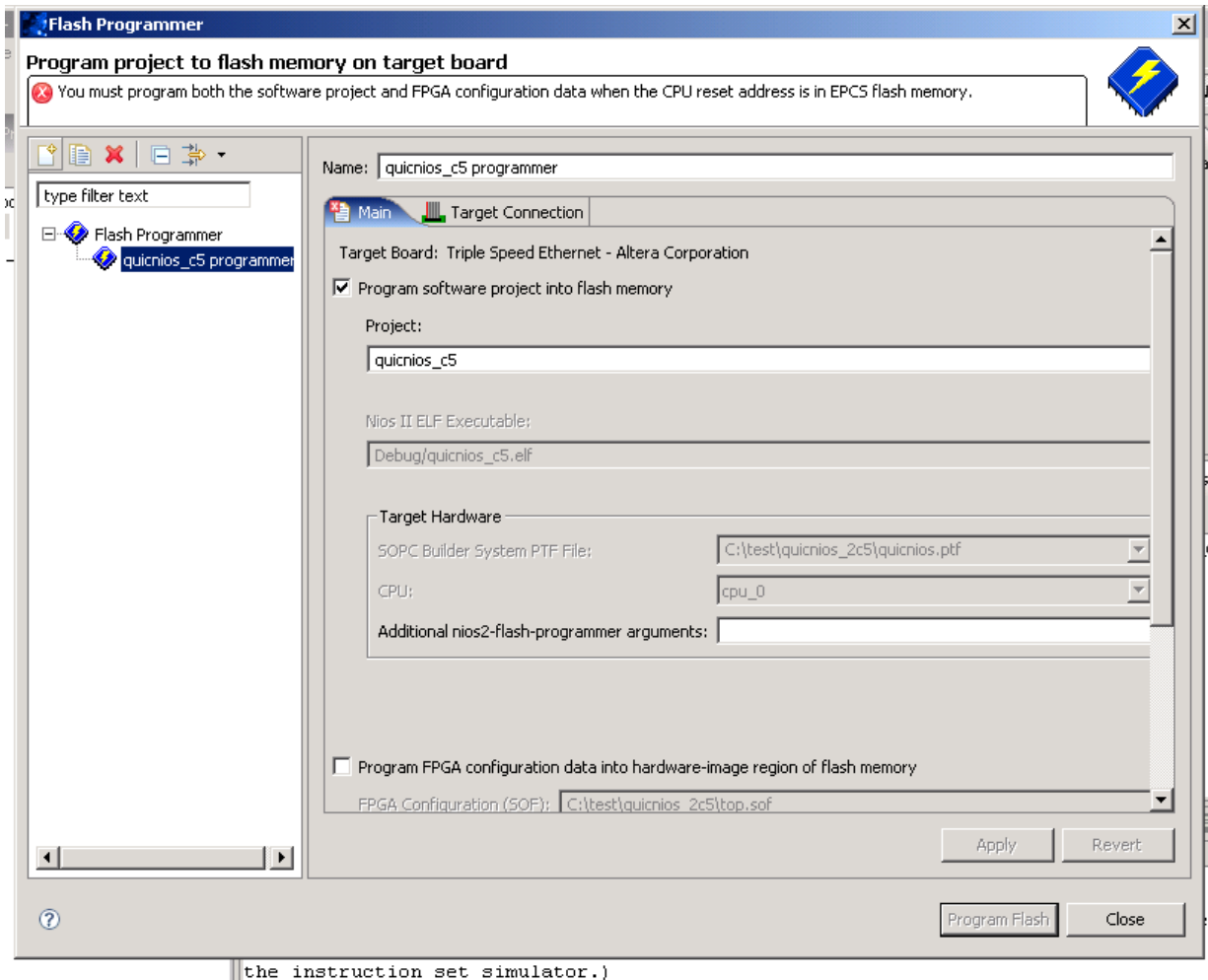
- From the “Tools” pull down select the Flash Programmer (shown below).



The window below should open.



- Press the “New Configuration” icon located at the top left of the flash programmer window, the window below should open.



Regarding the Target Board : Why does the target board report “Triple Speed Ethernet”

This is the original question and reply received from Altera support:

Question:

1) In version 6.0 we were still using board files that were selected in socp and then identified in the flash programmer as the "Target Board". Now that we do not select a board file in SOPC, I notice that the target board file in the flash programmer identifies the board as "Triple Speed Ethernet" even though my design does not include Ethernet at all. Is this just something left over from the earlier versions? The flash programmer operated correctly, so my guess is it was just a left over.

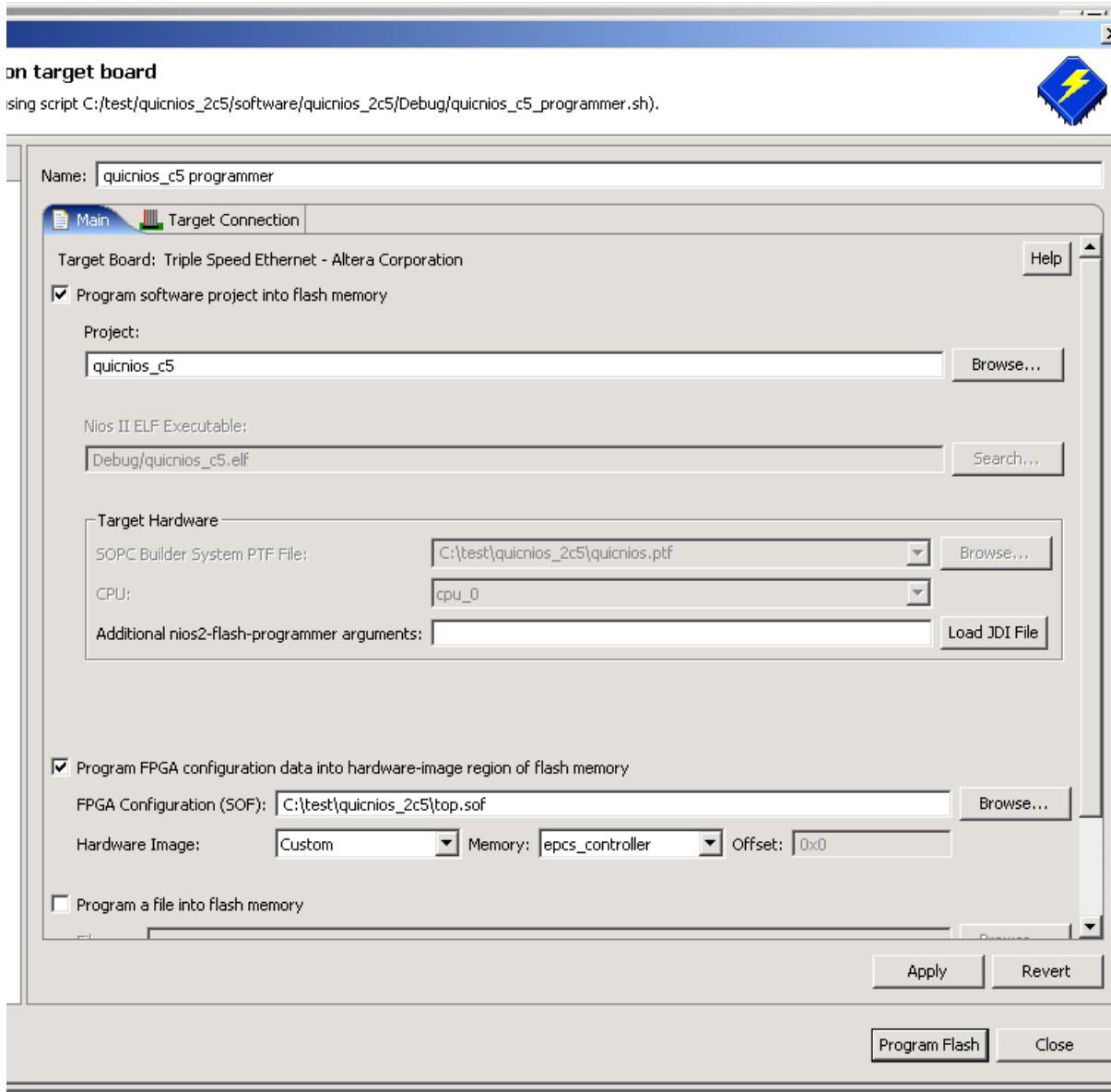
Answer:

Dallas Logic Corporation
 2300 McDermott Road • #200-305 • Plano, TX 75025
www.dallaslogic.com Ph. 972-359-2953

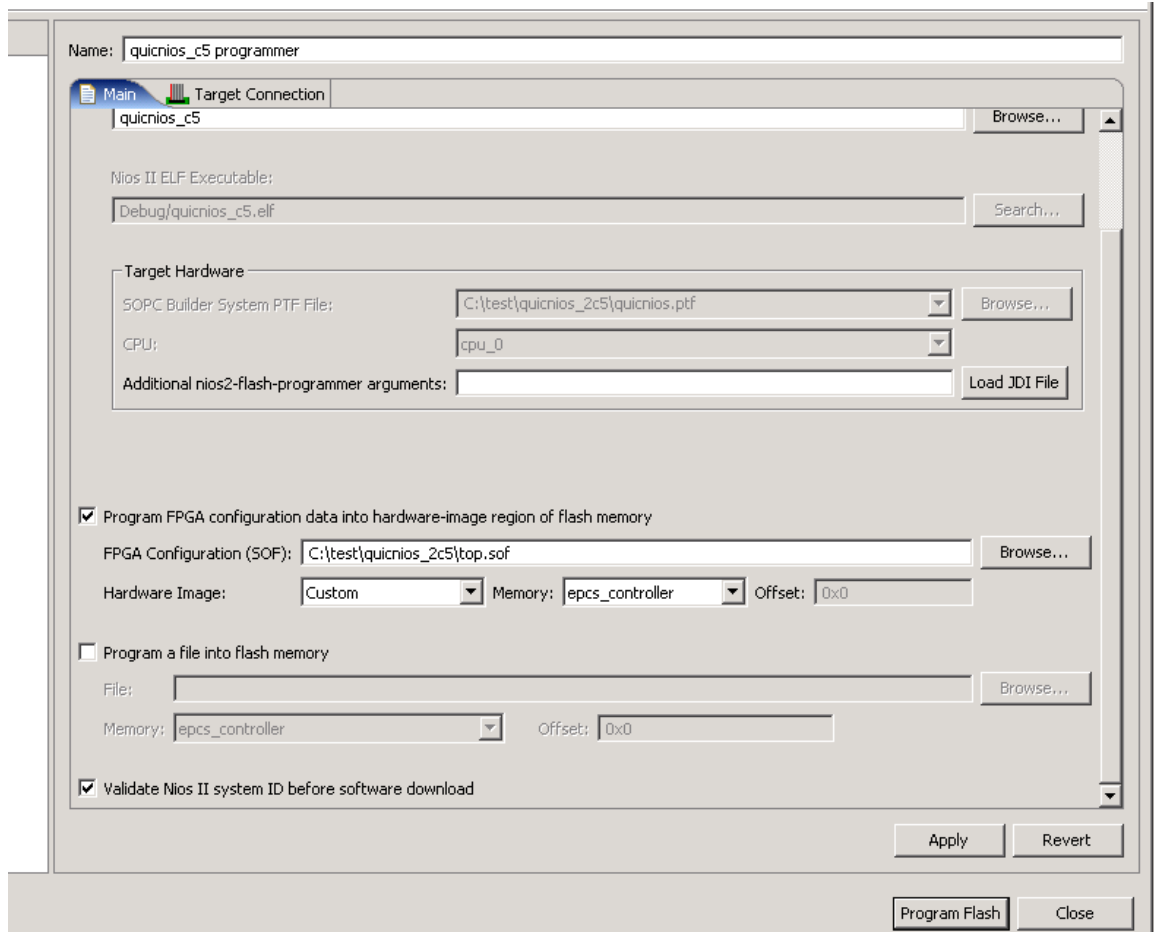
1. My guess is that this is something left over from the 6.0 version. Unfortunately, 7.2 no longer has the Make Target board feature since we have moved to using the Component Editor.

So ignore the target board reporting for version 7.2, this is a legacy feature that is no longer required / supported.

- Next, set up your flash programmer panel like the following two panels. Shown below are the top and bottom of a single panel. The entire window would not fit on a single screen shot.

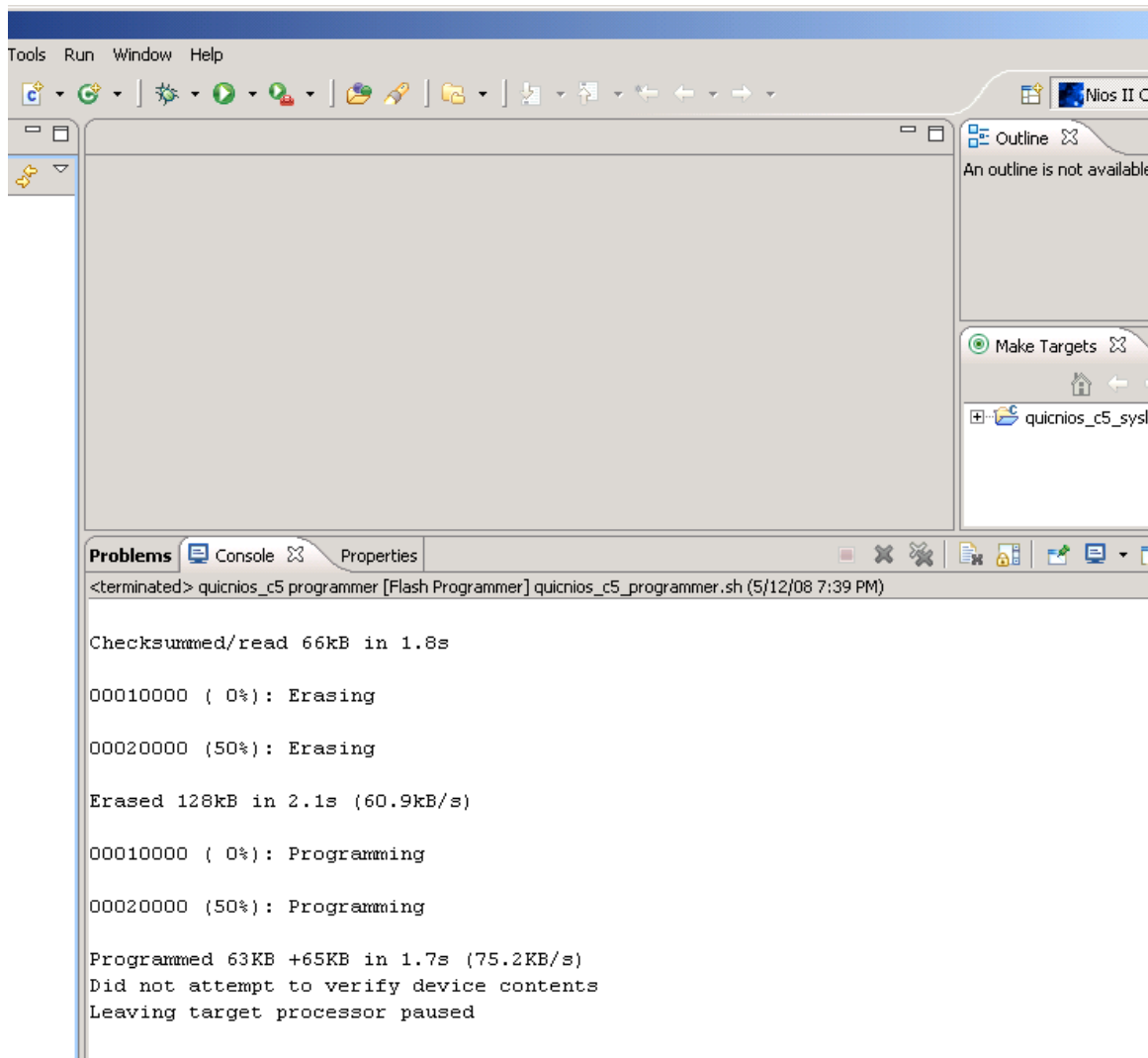


Bottom half of flash programmer



- Once your panel is setup press the “Program Flash” Button

After completing the Flash operation, you should see a similar message in the console window (shown below).



- Now remove the programmer from the JTAG header and Cycle Power. The NIOS II controller should begin cycling the LEDs.

More Questions?
Use the Dallas Logic Forums located at
<http://www.dallaslogic.com/forum/default.asp>

Dallas Logic Corporation
2300 McDermott Road • #200-305 • Plano, TX 75025
www.dallaslogic.com Ph. 972-359-2953