



Modular Circuit Specification



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Table of Revisions

Revision	Author	Date	Description
0.1	ET	12-22-05	First draft release of specification
1.0	ET	1-12-07	First release of specification
2.0	ET	3-09-09	Modification of document header/disclaimer. Change of VAUX0_5V power pins to 3.3V. Swap VAUX0 and 3.3V pin location. Increase maximum current on power pins to 2 Amperes. Addition of 0.12" (inch) to each side of module (Y dimension) to facilitate card guides. Addition of 0.02" to each end of modules (X dimension). Update diagrams to accurately show module dimensions. Edit pin mapping tables for clarity. Edge to edge module spacing on carrier set to 0.1" (from 0.2"). Added FIFO bus pin mapping to the expanded pin list.
2.1	ET	4-16-09	Improved serial bus mapping (MOSI, MISO, TX,RX, SSN, IRQ) so that input signals and output signals are grouped on the same pin type (input or output direction on any one pin).
2.11	ET	6-10-09	Increased module spacing from 0.1 inch to 0.12 inch on carrier.
2.12	JT	8-15-10	Added info on THR (through hole reflow), and updated disclaimer section.
2.13	ET	10-06-10	Added dimension for PCB center to center spacing on diagram pg. 38.

Preface

Cardstac™ is a specification for what is commonly termed SOM (System On Module). At the time of this writing (late 2005) there are a dozen or more SOM standards and product lines available from various manufacturers. Some of the available module products include:

- **PC/104™** by the PC/104 Embedded Consortium. ISA bus x86 embedded PC architecture using 140 pin pass-thru header (stackable). A widely used standard.
- **SOM-144** by Advantech. PCI and x86 architecture module supporting display, hard drive, USB, LPT, etc.
- **DIMM-PC®** and **X-board** by Kontron. PCI and x86 embedded PC architecture supporting numerous PC peripherals (VGA, hard-drive, USB, mouse, keyboard). Smaller SODIMM-144 form factor.
- **TINI®** By Dallas Semiconductor. Small micro-controller module for Internet based Java™ and TCP/IP control. Implemented on SIMM-72 and SODIMM-144 form factor PCB. Many manufacturers provide derivatives based on this standard.
- **E2Brain™** by Kontron. High performance module supporting several processor standards. Provides digital communications interfaces including UTOPIA. Inter-connect is provided by four Hirose FX8C series connectors. Cannot stack units (one unit per connector).
- **PC-MIP** is an ANSI standard which provides PCI based modules for use on PMC carrier cards.
- **M-Module** and **IndustryPack** are both ANSI standards for IO modules to be carried on mezzanine cards.
- **COM, AdvancedMC, AdvancedTCA** are the latest standards available from PICMG® (PCI Industrial Computer Manufacturers Group). For high-end “industrial strength” applications. COM is a processor module platform. AdvancedMC is a mezzanine card standard. AdvancedTCA is a system platform standard.
- **Gumstix™** by Gumstix inc. Provides numerous processor and expanded modules that connect using a Hirose type connector. Processor modules are capable of running Linux.
- **Heron** by Hunt Engineering. This is a module specification for DSP processing. Utilizes a FIFO type interface. Based on earlier GDIO and TIM-40 specifications.

More information about each of these standards can be found on the Internet. So why define another module standard? Although Cardstac modules can be defined as “systems” (CPU module for example), the modules are also intended as a test/inter-connect vehicle for individual IC devices or circuits. This is the primary difference as compared to other standards. In its physical implementation, Cardstac is a “simplest possible” solution (with respect to mechanical form factor, connectors, etc). Cardstac is

intended to support embedded processor architectures such as Atmel AVR®, 8051, TI MSP®, Altera Nios®, and ARM®. A design summary of the Cardstac specification is listed below.

- ❖ Standard module is credit card size (PCB). Specification also supports half-length modules for simple/compact functions. Module pin counts include 60, 128, and 256 pins.
- ❖ Simple rectangular mechanical outline and “low technology” 0.1 pin header inter-connect. Ideal for lab prototyping, testing, probing, and modification.
- ❖ Cardstac modules can be plugged together (stacked like PC/104™) or inserted into a carrier. Pin function “symmetry” allows connection in dual orientations (can support different functions).
- ❖ Cardstac provides a common, modular, inter-connect platform for testing IC products from various vendors.
- ❖ Module inter-connect pin definitions are driven by simple digital “hardware-level” device interfaces. Cardstac pin definitions are a mixture of digital interfaces commonly found on a single PCB design.
- ❖ Pin headers provide digital LVTTTL level interfaces only. Areas for on-module IO connectors are defined (for other interfaces such as RS-232, USB, Ethernet, CAN).
- ❖ Programmable logic devices are central to the design implementation (flexibility for interface definition, digital IP testing, ASIC prototyping).

The reader can review the other SOM standards for more detail. If the points summarized above support your design requirement, then read on. Hopefully, you will find Cardstac a useful tool for your own project!

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1 Introduction

Cardstac™ is a circuit specification for small, stack-able test and evaluation modules. These modules can be connected (stacked) as “building blocks” to form electronic systems with processing and IO capability. Cardstac modules are primarily intended for electrical educators, students, and designers as a vehicle for quickly testing and prototyping electronic devices and circuits. Manufacturers can also utilize the modules to reduce design and debug effort for low volume or short lead-time products.

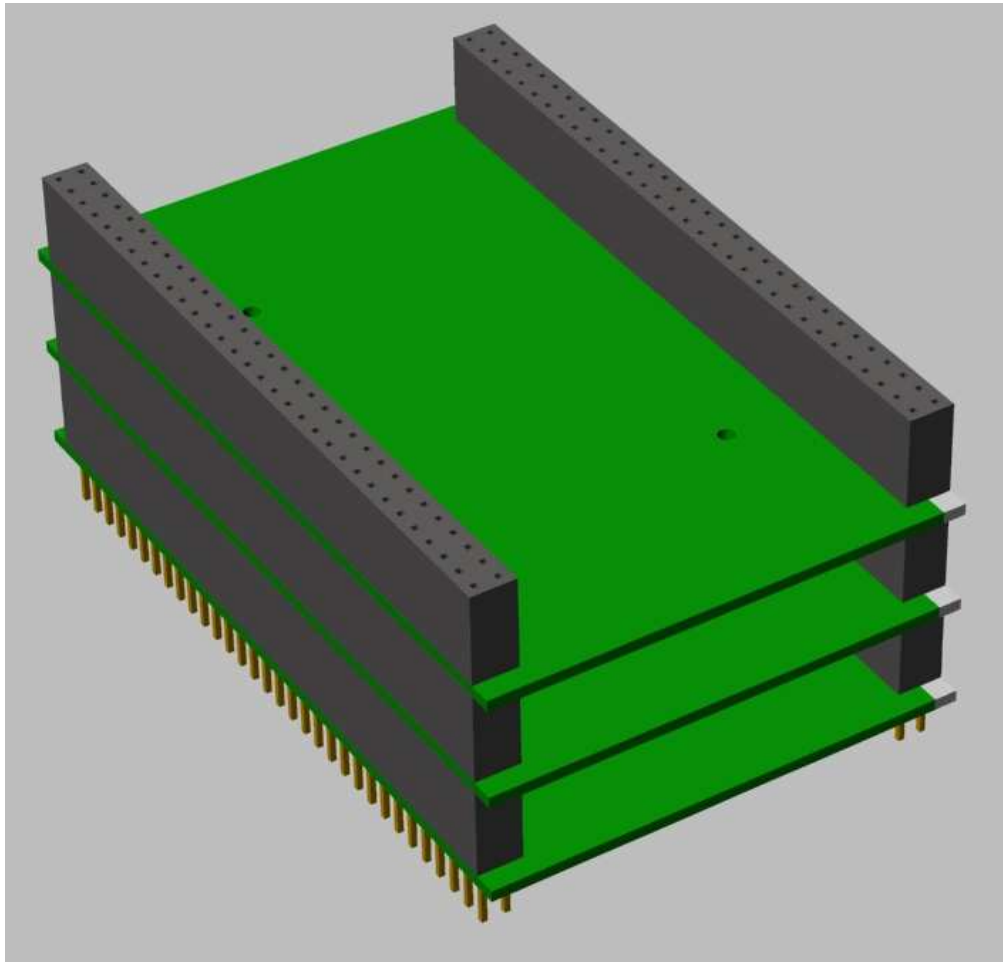


Figure 1: Cardstac Example

This specification is mainly inspired by the PC/104™ specification. PC/104™ is an ISA bus based standard for the embedded PC market, and provides a definition for circuit module interconnect, form-factor, and power. Unlike the PC/104™ specification, which targets a specific bus interface, Cardstac is for a wider mix of circuit types. This will certainly result in compatibility issues between specific Cardstac families. FPGA and PLD devices can provide added flexibility in IO compatibility as power pin positioning is always maintained and FPGA devices can provide custom IO mapping. Cardstac, at a minimum, provides a standard mechanical form-factor and power pin definition. The recommended IO

pin mapping provides common digital communication interfaces and is flexible in its implementation. Cardstac does not directly define high speed IO or specific IO PHY types (USB, Ethernet, RS-232). System IO can be implemented on a dedicated IO card within a Cardstac system. High-speed connectors and specific IO connector types are implemented within dedicated PCB areas (right and left end of PCB card). Cardstac modules can be used for:

- Evaluation of IC devices and new circuits.
- Testing of digital IP (intellectual property) and ASIC prototyping.
- Design cycle reduction (through replication of module design and documentation into new designs).
- Short lead-time products.

2 Cardstac Basics

Cardstac provides guidelines for the following design parameters:

- **Pin Inter-connect:** Simple 0.1 inch pitch pin headers are utilized in 256, 128, and 60 pin counts. Provide common digital interfaces in standardized pin locations. Pin mapping symmetry and “pass thru” pin headers allow for module stacking and rotation. Carrier cards can also be utilized to provide pin inter-connect.
- **Card Size:** A credit card provides ample space for a minimal design, and most of us have a handy size reference in our pocket (standard card). Half size cards are also defined.
- **Card Power:** 3.3V and one auxiliary power rail (VAUX0_+12V) are provided. A current limit of two Amperes is set for each 0.10 pitch header pin. The +3.3V voltage rail is therefore limited to eight Amperes in a standard card stack (four +3.3V pins), and the VAUX0 rail is limited to four Amperes (two pins).

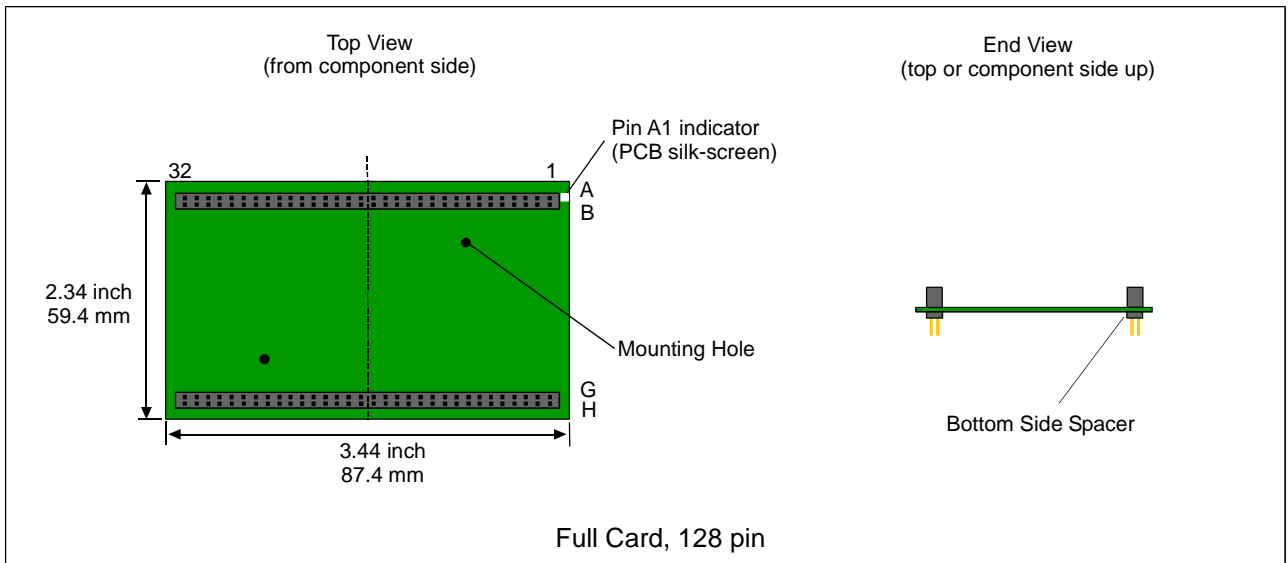


Figure 2: Cardstac Module General Details

Cardstac digital interconnect is typically provided by two 64 pin 0.10 inch pitch pin headers for a total of 128 pins (standard size card). These two 64 pin connectors provide four rows of pins labeled as rows A, B, G, and H (rows C, D, E, and F are expanded rows, and are only used on 256 pin cards). Although a very “low tech” connector, 0.10 inch pitch pin headers have the advantage of low cost, easy access for probing, and low PCB technology requirements. Pin headers also attach directly to 0.10 inch pitch proto-board, can use ribbon cable, and can also be wire-wrapped.

The PC/104™ standard uses one 64 pin and one 40 pin “pass-thru” connector with 0.80 inch or 0.60 inch connector height. This connector height results in a very thick stack for a smaller module size. Cardstac cards are “credit card” size, and are roughly half the size of a PC/104™ card. Cardstac modules use 0.435 inch (11.05 mm) board to board spacing. Therefore, there is less clearance on a PCB for “tall” components (as compared to PC/104™). This will not apply if the component is located on the top card in the stack (optimal position for IO cards). Note that 0.1 inch (2.54 mm) thick plastic pin spacers can be used to increase module to module spacing if necessary.

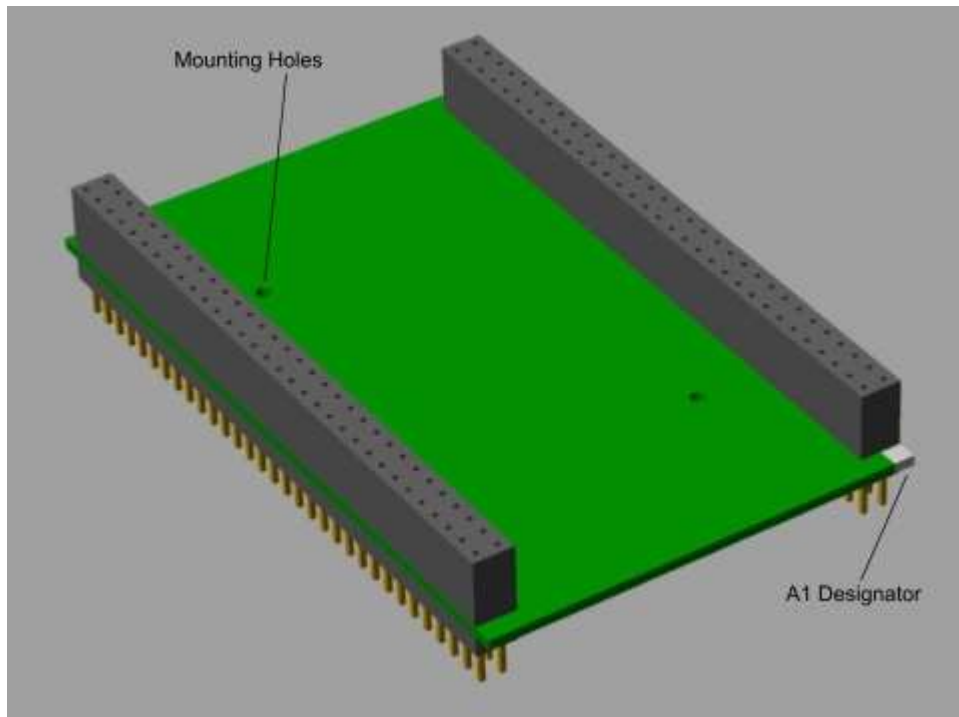


Figure 3: Example Cardstac Module (no components)

The open ends of a Cardstac module are free of tooling holes to allow maximum placement space for right-angle power and IO connectors. Modules that are mounted only on the top of a stack (or on a carrier) can also have vertical IO connectors on the PCB. Two mounting holes are located centrally to the PCB, and provide stability for both standard and half cards (when secured with a stand-off and screw). These holes also indicate proper card orientation for half cards.

A Cardstac system (stack) does not contain orientation card guides or connector keys. Users must visually verify proper Pin A1 and mounting hole orientation before connecting (stacking) Cardstac cards. Pin A1 should always be marked with a white silk-screen square or dot on both standard and half cards. The pin A1 PCB silkscreen indicator should always be placed on the **top-side** (component side) of the PCB only. The A1 indicator must always be on the same PCB side for all cards connected in a stack.

3 Master and Slave Modules

Cardstac modules are defined as being **master** or **slave** types. Each Cardstac system can have one master and multiple slave cards. The master card in a stack defines:

- The default control element (microprocessor or state-machine).
- The stack A1 pin location
- The drive direction of electrical signals (input or output with respect to master card)
- The location of pull-up resistors for open-collector/open-drain signals.

Other cards in a stack can still be assigned control functions following initialization. Arbitration for and assignment of stack control is outside the scope of this specification. Power is not necessarily provided by a master card. If no true control element is present in a design, signal IO direction is still defined with respect to a designated master card.

It is recommended that master modules and slave modules be labeled to allow easy identification of the card type. This can be done by adding a suffix to the module part-number. For example:

- XXXXX-M denotes a master card.
- XXXXX-S denotes a slave card.
- XXXXX-MS denotes a dual function master or slave card.

4 Form-factor Types

There are six basic form-factor types defined by the Cardstac specification. Each module type is shown in the figure on the next page. Careful consideration of the available pin mapping should be made before selection of a form factor type. Each form-factor type is numbered below.

1. Standard Card (64x2): This module type is the **default configuration** and provides 128 pins. This configuration will allow all pins to “pass-thru” in a stacked configuration.
2. Half Card (30x2): This module type is a **half configuration** and provides 60 pins. Modules are rotated when inserted on either end of a standard card (tooling holes always line up). Note that standard card pins 16 and 17 are not connected on half cards (these pins do not exist on half cards).
3. Standard Card (64x1 single connector): The standard “SC” module type provides rows G and H on one side of the card only, providing 64 pins. This configuration can be used for vertical installation into a card carrier (using right angle connector). The empty side of the card (rows A and B absent) provide areas for custom connectors or signal probe headers.
4. Half Card (30x1 single connector): The half “SC” module type provides rows G and H on one side of the card only, providing 30 pins. A card of this type has a minimal address/data bus only (digital pin mapping).
5. Expanded Card (64x4): This module type provides an additional four pin rows (C, D, E, F) for 256 pins total. Note that rows C, D, E, F are replications of A, B, G, H with respect to power and ground placement. Used for high IO count applications. This card type could be used to provide a bridge between two isolated 128 pin standard cards, or an interface between a 128 pin card and external circuits.
6. Half-expanded Card (30x4): This module type provides standard and expanded rows (A, B, C, D, E, F, G, H) in a half card configuration for 120 pins total.

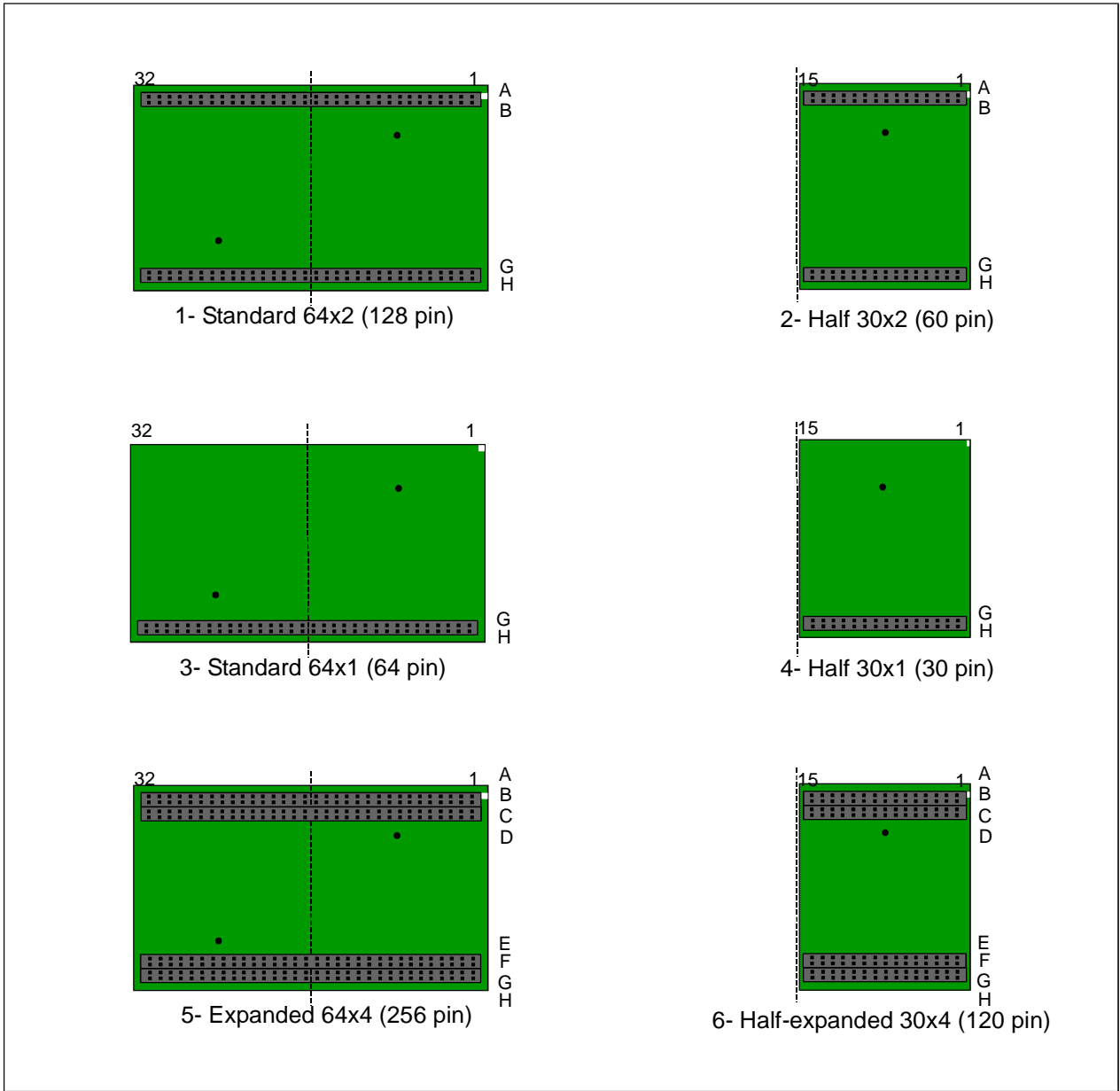


Figure 4: Form Factor Types

5 Inter-connect Types (Carriers)

Cardstac supports module inter-connect directly via stacking. Another option is the use a carrier card to provide module power and pin inter-connect. Because of the low density of Cardstac connectors and bus geometry of the signals, a simple, low technology PCB should be adequate for most carrier card designs. Carriers have an advantage for some applications that include:

- Easier access to, and modification of card selection during testing.
- End product that benefits from a carrier form-factor.
- Control/interfacing of isolated bus groups on a carrier through a “bridge” module.
- For a vertical mount carrier (right angle connector used for module row GH), the AB side of a module is open, and can be used for IO connector placement or signal monitoring.
- For a horizontal mount carrier, the center area of a module PCB can be used for vertical IO connectors (instead of the end areas only).

Inter-connect configurations are classified into six type groupings (type 1, 2, 3, 4, 5 and 6). These inter-connect types are shown in the figure located on the next page.

1. **Horizontal Stack:** Inter-connect without a carrier using the module pins only. This is the simplest method for interconnecting modules. Card to card clearance (for components) is limited by the stacking connector height.
2. **Horizontal Carrier:** PCB used to inter-connect two or more horizontal stacks of Cardstac modules. All signals are connected on a single parallel bus (signals connected directly together just like a stack).
3. **Horizontal Carrier (multi-bus):** PCB used to inter-connect two or more horizontal stacks of Cardstac modules. Two or more isolated bus groups exist. Bus groups can be bridged by a module located centrally to the carrier. The central module is used to provide control functions or interface functions for the separate bus groups located to each side of the module.
4. **Vertical Carrier:** PCB used to inter-connect two or more Cardstac modules using right angle connectors. This allows a single module to support dual circuit functions (either side of module can be inserted). Also provides for module interconnect on one side, and signal monitoring or custom IO on outer side.
5. **Hybrid Carrier:** PCB used to inter-connect both horizontal Cardstac modules and vertical modules using right angle connectors. All signals are connected on a single parallel bus (signals connected directly together just like a stack).
6. **Hybrid Carrier (multi-bus):** PCB used to inter-connect both horizontal Cardstac modules and vertical modules using right angle connectors. Two or more isolated bus groups exist and can be bridged by a centrally located module. The central module is used to provide control functions or interface functions for the separate bus groups located to each side of the module.

Top View
(from component side)

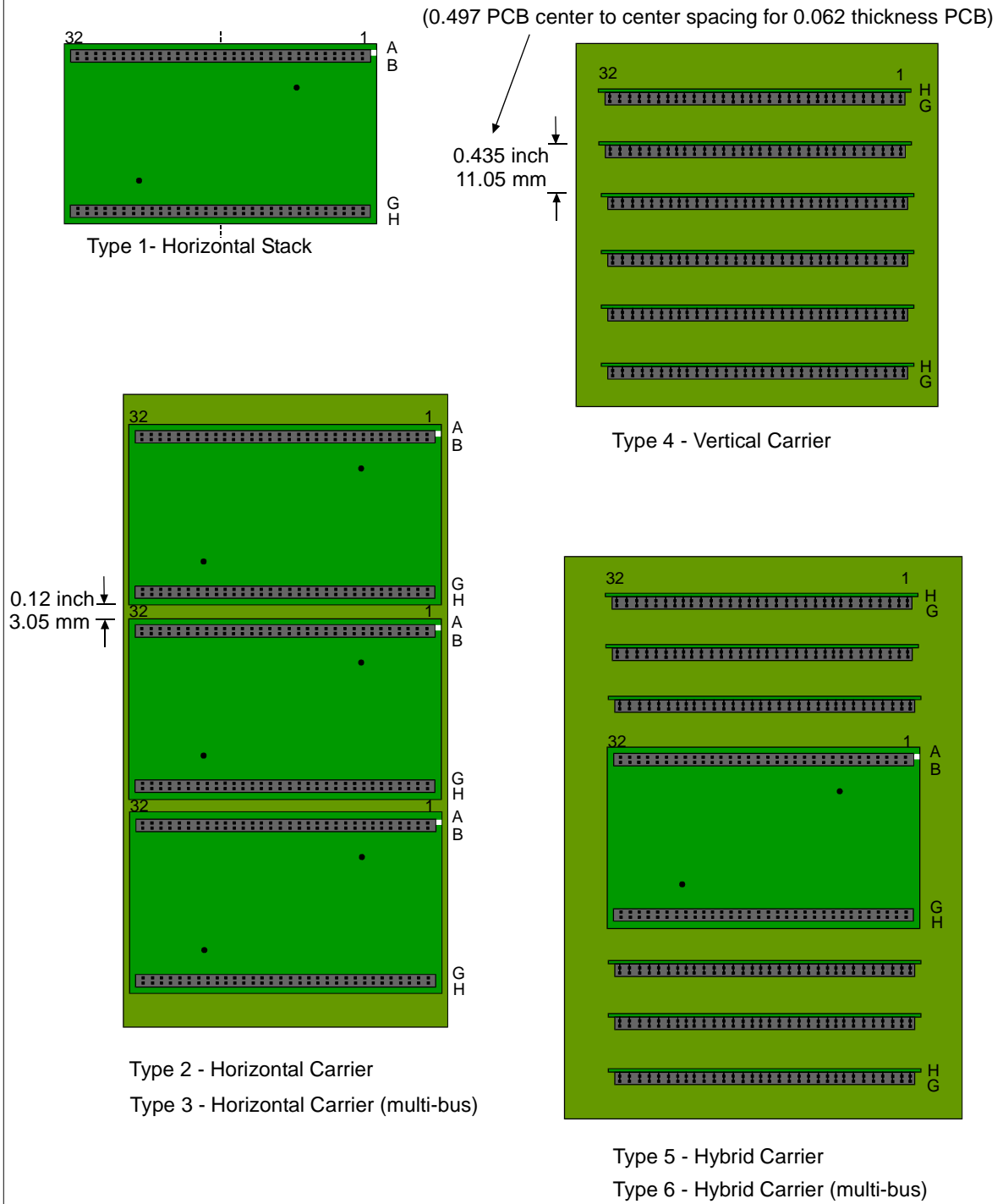


Figure 5: Inter-connect Methods (types)

Carriers (and enclosures) can be developed with many variations in size and geometry. Carriers might only provide basic functions such as power and module inter-connect, or additionally, could provide processors or other active circuits. Although this specification does not cover carriers in detail, by adhering to some basic geometry guidelines, carrier variation can be minimized and options for inter-connect are maximized. To minimize variation in carrier geometry, the following carrier module spacing is recommended:

- **Horizontal Carriers:** should use a module PCB “edge to edge” spacing of 0.12 inch (3.05 mm). Refer to Figure 5 for an indication of this spacing. By standardizing this spacing, “double width” cards can be designed which span multiple standard card positions. A “double card” can be used for implementing circuits that will not fit on a standard size card. This spacing (0.12 inch) should not be increased or decreased.
- **Vertical Carriers:** should use a module PCB “surface to surface” spacing of 0.435 inch (11.05 mm). For a 0.062 thick module PCB, the resulting “center to center” module PCB spacing will be 0.497 inch (12.6 mm). This dimension is the same spacing used for modules in a stack, and is based on the height of the pin connector and spacers (see section on mechanical dimensions). Maintaining this same PCB spacing will allow a module pair to be interconnected with a standard height pin connector on one side of the pair (using vertical module connector), and still be plugged into a vertical carrier when two right-angle connectors are installed on the other side of the card pair. This “surface to surface” dimension (0.435 inch) can be increased if greater spacing is desired (for increased component height or better air-flow). This spacing should not be decreased.

6 Pin Header Types

Some thought must be given to the type of pin headers used to connect (stack) a Cardstac system. The selected pin-header type will define how a stack can fit together. Two groupings of pin header types are defined as **standard**, and **right-angle**.

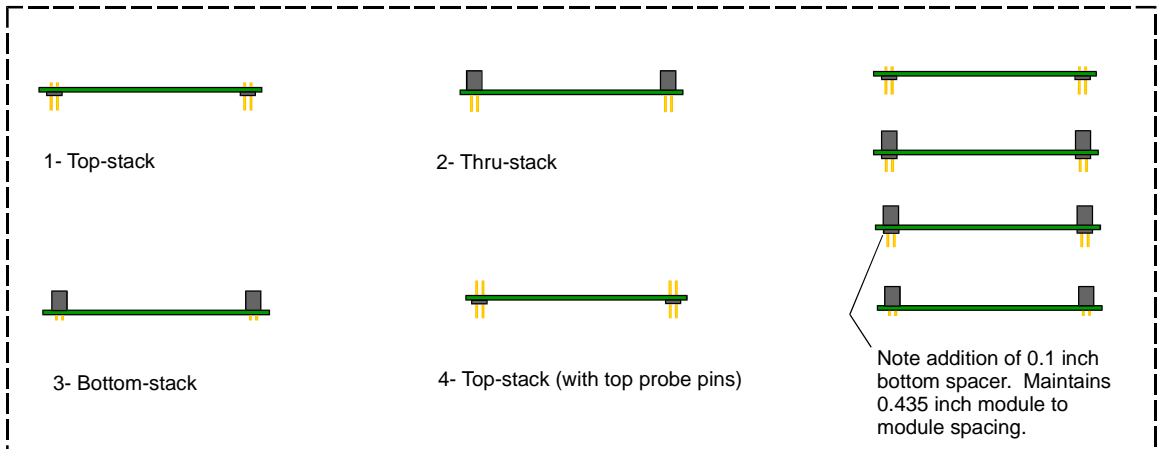
- **Standard:** includes types 1,2,3 and 4 headers or socket strips. These connectors are used for general stacking of modules.
- **Right-angle:** includes types 5 and 6 pin headers or socket strips. Used for mounting Carstac modules on vertical carrier boards. Allows an active bus to run on the carrier PCB, while IO pins (or probe points) are accessed on the free module side.

“Low insertion force” (LIF) socket strips/female connectors are recommended. If not used, the amount of force that is required to press cards together (stack) or remove cards can be excessive. This is due to the high number of pins on the connector. Connectors with spacers should have an overall height of 0.435 inch (11.05 mm) to provide correct spacing (surface to surface of PCB). The figure on the next page shows the different pin header types used with Cardstac modules.

End View of Card

(Top or component side is up)

Standard Header Types



Right Angle Header Types

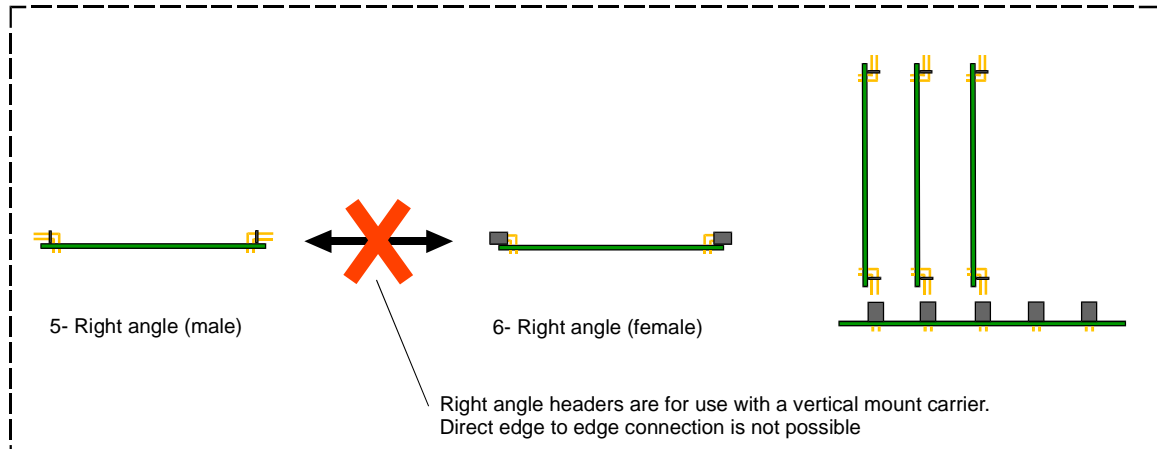


Figure 6: Pin Header Types

7 Standard and Half Card Stack Orientation

The two mounting holes on the Cardstac PCB indicate the correct card orientation for standard and half cards. **Standard cards** can be stacked either with pin A1 aligned (A1 orientation), or A1 rotated away by 180 degrees (H32 orientation). When rotated by 180 degrees (H32 orientation), proper power and ground pin connection will be maintained, but IO pin signal direction is not guaranteed (depends on selected function of some dual purpose pin). This capability provides for dual-purpose cards where a single card might provide two different interface types depending on rotation. Note that the default orientation is such that pin A1 aligns on all cards (with 180 degree rotation as the option).

Half cards are connected to a standard card with A1 or H32 orientation. Proper ground, power, and pin signal direction are always maintained (when using standard pin functions). The center pins (row 16 and 17) of a standard card are not connected to half cards. The mounting holes for half/standard cards should always line up in a stack. Do not insert half cards shifted to the right or the left on a host standard card. Always insert a half card with A1 aligned to A1 on the host card or A1 aligned to H32 on the host card. IO connectors will always face outwards when using half cards (in both A1 and H32 orientation) if IO connectors are only placed on the A1 end of half cards.

The pin A1 PCB silkscreen indicator should always be placed on the **top-side** (component side) of the PCB only. The A1 indicator must always be on the same PCB side for all cards connected in a stack.

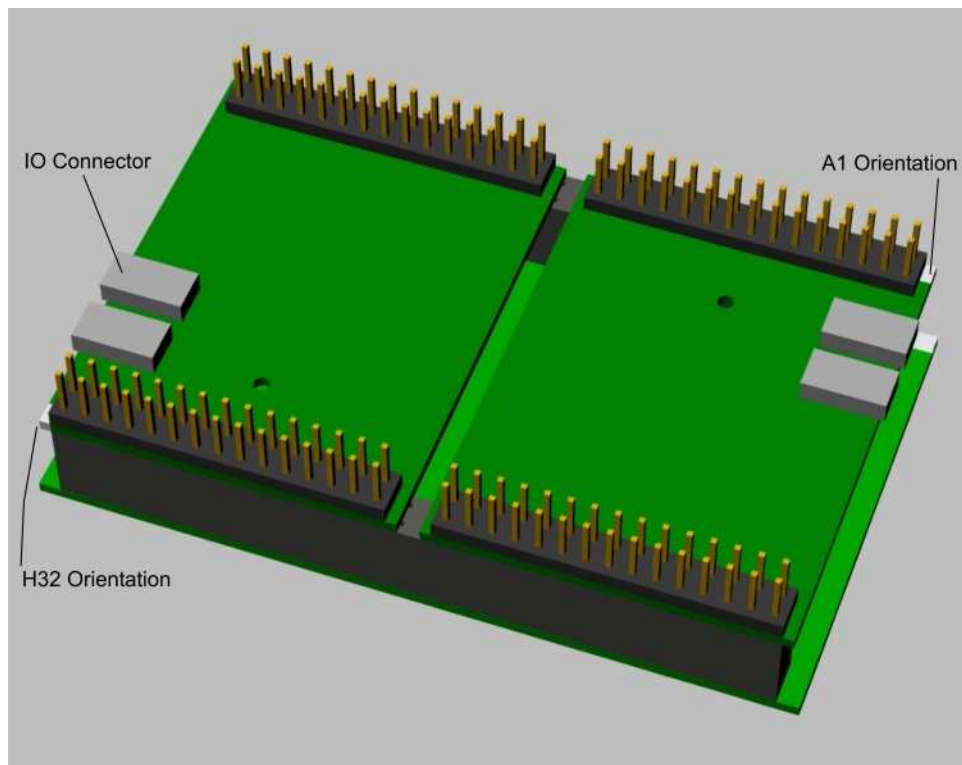


Figure 7: Half Cards Mounted to Standard Card

8 Pin Function Mapping

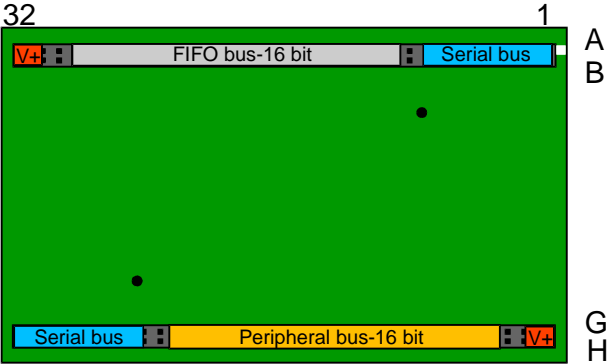
The pin mapping of Cardstac IO pins provides communications interfaces as found in a typical digital system. The pin mapping can be broken down into required pins (power, ground, and basic control signals) and recommended pins (digital interfaces). The following table shows the signal and power pin counts for each type of card.

Table 1: Pin Count By Type

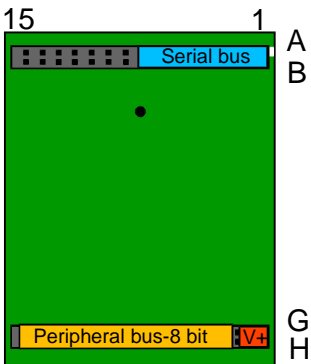
	Power Pins	Ground Pins	Signal Pins	Total Pins
Half Card	3	6	51	60
Standard Card	6	12	110	128
Expanded Card	12	24	220	256

Recommended digital interfaces also have functional groupings, of which some functions can be omitted to allow for other interface types. The signal grouping for Cardstac pins is shown in the figure on the next page.

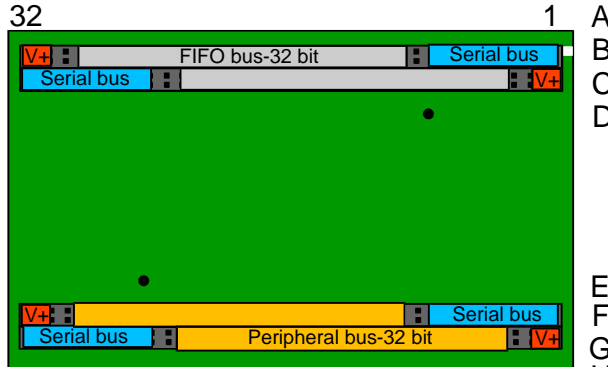
Cardstac Functional Pin Grouping



Standard 16 bit pin grouping (128 pin card)

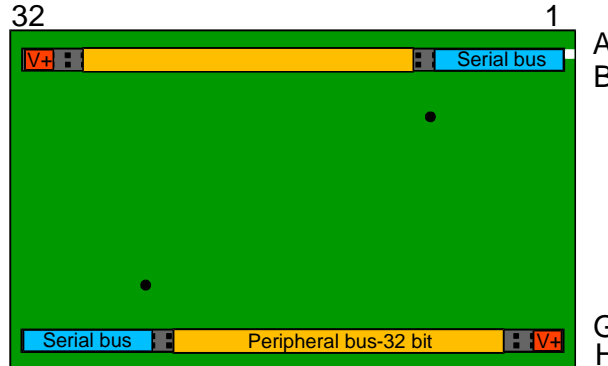


Half card pin grouping (60 pin card)



Expanded 32 bit pin grouping (256 pin card)

Expanded pin grouping defines pins in addition to standard pin grouping.



Alternate 32 bit pin grouping (128 pin card)

Alternate pin grouping is defined as a substitution for standard pin grouping. It is for designs that require a 32 bit peripheral bus on a 128 pin card.

Figure 8: Cardstac Functional Pin Grouping

Omitting one of the standard digital interfaces and replacing it with a custom interface **might** cause a Cardstac module to be incompatible with other Cardstac products. Custom selection of interface type is necessary for flexible implementation of Cardstac systems, and is important for a design/test environment. Still, by following some basic mapping guidelines general compatibility (perhaps with very slight modification) can be maintained and is considered adequate for prototype and test applications. Use of EPLD/FPGA devices where possible will also add flexibility to interface pin mapping.

Cardstac pin mapping is logically grouped to two sides of the card (rows A, B and rows G, H). There is also symmetry of signal groups with respect to the two ends of the cards to support the installation of half cards on a host standard card. Rows G, H support a primary memory mapped peripheral bus, and rows A, B support a synchronous digital FIFO type interface (or a secondary memory mapped peripheral bus with similar pin function mapping).

Half cards placed at each end of a standard card will pick up power pins, clock and reset signals, serial interfaces, and a subset of the peripheral IO bus (address, data, read, write). Interrupt signals on standard cards are broken up into group A and B. Group A interrupts are available for H32 oriented half cards (interrupts located on rows GH), and Group B interrupt are available for A1 oriented half cards (interrupts located on rows AB). The reset signal can be driven to or driven by slave peripheral devices (open collector signal). This implies that reset should be bidirectional on the master board so that it can drive or read the status of the reset signal. This allows the master control element to drive reset to the system for initialization. A separate reset signal for the Master control element (local to the master board only) should be provided. This allows a system wide reset which will not cause a reset of the master controller.

Serial/interrupt pin mapping is shown as an example in the table below (for the GH corner of the module). The serial port mapping operates the same way at both ends of a standard 128 pin module (serial/interrupt port groups are located top of rows AB and bottom of rows GH). Note that serial/interrupt pin mapping aligns input direction and output direction functions. The default mapping will provide one I2C port, four SPI ports, and four interrupt pins. If a UART TX/RX type serial port is to be utilized, then the number of SPI ports and interrupts must be reduced by one. If two UART serial ports are to be utilized, then 2 interrupts and two SPI ports are available. Using RTS/CTS (Request to Send/Clear to Send) handshaking on the UART serial ports will further reduce the available SPI/interrupt ports to one or zero (hand-shaking on one or both UART serial ports). When no SPI ports are available, a third UART TX/RX serial port can be implemented on the SPI_MISO and SPI_MOSI pins (no RTS/CTS signaling available for the third UART port). RTS and CTS are generally used when a UART serial port requires hardware level (instead of software level) synchronization due to high speed. The I2C serial port does not have a secondary function.

Table 2: Serial Pin Functions for Rows GH (replicated on upper portion of AB)

PIN	PRIMARY IN	SECONDARY IN
H28	IRQ0A-	0CTS
H29	IRQ1A-	1CTS
G24	IRQ2A-	0RX
G25	IRQ3A-	1RX
G30	0SPI_MISO	2RX
PIN	PRIMARY OUT	SECONDARY OUT
G26	0SPI_SSN0-	0RTS
G27	0SPI_SSN1-	1RTS
G28	0SPI_SSN2-	0TX
G29	0SPI_SSN3-	1TX
G31	0SPI_MOSI	2TX
G32	0SPI_CLK	
H30	0I2C_SDA (bidir)	
H31	0I2C_SCL	

The three tables on the following pages show recommended Cardstac pin mapping. The color highlighting is defined by:

- **Yellow:** required pins to support baseline Cardstac compatibility. Power, ground, reset, and clock pins.
- **Gray:** Indicates the synchronous digital FIFO interface (or can be used as a secondary 16 bit memory mapped peripheral bus).

Pin signal direction (input or output) is defined with respect to a stack “master card” which is the primary control element. **Therefore, on a slave card, the signal direction would be reversed.** The three tables on the following pages indicate:

- **Standard Pin Mapping (16 bit):** Standard pin mapping is the recommended pin-out for a standard-length 128 pin card (rows A, B, G, H). This mapping provides a single 16 bit asynchronous IO bus and another separate 16 bit synchronous FIFO type bus as well as several serial interfaces. A secondary 16 bit IO bus can be substituted for the synchronous FIFO bus. The standard Cardstac pin-out provides 17 address bits for 128Kx16 address range with five separate chip selects (CS0- to CS4-). Byte enables should be mapped to ADD15 and

ADD16 if required (BE0- and BE1-). Using byte enables would result in a 32K x 16 byte addressable range. Note that this memory range is for peripheral devices. Memory store (SRAM, DRAM) should be located on a separate bus locally to the processor.

- **Expanded Pin Mapping:** Expanded pin mapping adds an extra 128 pins (rows C, D, E, F) to standard pins (rows A, B, G, H) for 256 pins total. Expanded pin mapping is a replication of the standard 128 pin mapping for power and ground nets. The expanded signal definitions add a 32 bit peripheral bus as well as a 32 bit FIFO bus. Additional address and status bits are also added, as well as more serial IO interfaces. Pins which are not defined can be used for custom IO. Note that for bridging functions, an expanded card might implement two of the same type interface (peripheral or FIFO bus) on each side of the module.
- **Alternate Pin Mapping (32 bit):** Alternate pin mapping is a possible substitute for the standard pin format (rows A, B, G, H). Alternate pin mapping should only be used in cases where a 32 bit peripheral bus with individual byte enables is required for a 128 pin card form factor. Twenty eight address bits and four separate byte enables (BE0-, BE1-, BE2-, BE3-) are provided.

There will be design cases where a few extra general purpose IO lines are required (things just wont fit into the standard pin definition). The upper eight bits of each data bus are the “recommended” location for placing general purpose IO. The result of this pin definition change is the corresponding data bus (peripheral or FIFO) will be reduced to an 8 bit bus, rather than 16 bit. The peripheral bus general IO locations are labeled as IO bus A, and the FIFO bus general IO locations are labeled as IO bus B. The FIFO bus location (IOB) should be utilized for general purpose IO first, as hardware based FIFO bus designs will generally be less prevalent.

Table 3: Cardstac Standard Card Pin Mapping (16 bit)

PIN	ROW A	ROW B	ROW G	ROW H
1	GND	1SPI_CLK	VAUX0 / +12V	+3.3V
2	I2C_SCL	1SPI_MOSI/5TX	+3.3V	GND
3	I2C_SDA	1SPI_MISO/5RX	CS0-	RST-
4	IRQ5B- / 4CTS	1SPI_SSN3-/4TX	CS1-	ADD0
5	IRQ4B- / 3CTS	1SPI_SSN2-/3TX	CS2-	ADD1
6	S-CLK4	1SPI_SSN1-/4RTS	CS3-	ADD2
7	GND	1SPI_SSN0-/3RTS	CS4-	CLK0
8	S-CLK3	IRQ7B- / 4RX	DATA0	GND
9	S-DP1	IRQ6B- / 3RX	DATA1	WRITE-
10	S-DP0	S-D15 / IO7B	DATA2	ADD3
11	S-STAT9	S-D14 / IO6B	DATA3	ADD4
12	S-SYNC-	S-D13 / IO5B	DATA4	ADD5
13	GND	S-D12 / IO4B	DATA5	READ-
14	S-CLK2	S-D11 / IO3B	DATA6	GND
15	S-STAT8	S-D10 / IO2B	DATA7	ADD6
16	S-STAT7	S-D9 / IO1B	DATA8 / IO0A	ADD7
17	S-STAT6	S-D8 / IO0B	DATA9 / IO1A	ADD8
18	S-CLK1	S-D7	DATA10 / IO2A	ADD9
19	GND	S-D6	DATA11 / IO3A	ADD10
20	S-READ-	S-D5	DATA12 / IO4A	GND
21	S-STAT5	S-D4	DATA13 / IO5A	ADD11
22	S-STAT4	S-D3	DATA14 / IO6A	ADD12
23	S-STAT3	S-D2	DATA15 / IO7A	ADD13
24	S-WRITE-	S-D1	IRQ2A- / 0RX	ADD14 /WAIT-
25	GND	S-D0	IRQ3A- / 1RX	ADD15 /BE0-
26	CLK1 (S-CLK0)	S-SEL4	0SPI_SSN0-/0RTS	GND
27	S-STAT2	S-SEL3	0SPI_SSN1-/1RTS	ADD16 /BE1-
28	S-STAT1	S-SEL2	0SPI_SSN2-/0TX	IRQ0A- /0CTS
29	S-STAT0	S-SEL1	0SPI_SSN3-/1TX	IRQ1A- /1CTS
30	RST-	S-SEL0	0SPI_MISO/2RX	0I2C_SDA
31	GND	+3.3V	0SPI_MOSI/2TX	0I2C_SCL
32	+3.3V	VAUX0 / +12V	0SPI_CLK	GND

Table 4: Cardstac Expanded Card Pin Mapping (in addition to standard pins)

PIN	ROW C	ROW D	ROW E	ROW F
1	VAUX1	+3.3V	GND	2SPI_CLK
2	+3.3V	GND	2I2C_SCL	2SPI_MOSI/8TX
3	S-SEL5		2I2C_SDA	2SPI_MISO/8RX
4	S-SEL6	S-STAT10	IRQ9C- / 7CTS	2SPI_SSN3-/7TX
5	S-SEL7	S-STAT11	IRQ8C- / 6CTS	2SPI_SSN2-/6TX
6	S-SEL8	S-STAT12	WAIT-	2SPI_SSN1-/7RTS
7	S-SEL9	CLK3 (S-CLK5)	GND	2SPI_SSN0-/6RTS
8	S-D16	GND	ADD27	IRQ11C- / 7RX
9	S-D17		ADD26	IRQ10C- / 6RX
10	S-D18	S-STAT13	ADD25	DATA31
11	S-D19	S-STAT14	BE3-	DATA30
12	S-D20	S-STAT15	BE2-	DATA29
13	S-D21		GND	DATA28
14	S-D22	GND	BE1-	DATA27
15	S-D23	S-CLK6	BE0-	DATA26
16	S-D24	S-STAT16	ADD24	DATA25
17	S-D25	S-STAT17	ADD23	DATA24
18	S-D26	S-STAT18	OE-	DATA23
19	S-D27	S-CLK7	GND	DATA22
20	S-D28	GND		DATA21
21	S-D29		ADD22	DATA20
22	S-D30	S-STAT19	ADD21	DATA19
23	S-D31	S-DP2	ADD20	DATA18
24	IRQ14D- / 9RX	S-DP3		DATA17
25	IRQ15D- / 10RX	S-CLK8	GND	DATA16
26	3SPI_SSN0-/9RTS	GND	CLK2	CS9-
27	3SPI_SSN1-/10RTS	S-CLK9	ADD19	CS8-
28	3SPI_SSN2-/9TX	IRQ12D- /9CTS	ADD18	CS7-
29	3SPI_SSN3-/10TX	IRQ13D- /10CTS	ADD17	CS6-
30	3SPI_MISO/11RX	3I2C_SDA		CS5-
31	3SPI_MOSI/11TX	3I2C_SCL	GND	+3.3V
32	3SPI_CLK	GND	+3.3V	VAUX1

Table 5: Cardstac Alternate Pin Mapping (32 bit)

PIN	ROW A	ROW B	ROW G	ROW H
1	GND	1SPI_CLK	VAUX0 / +12V	+3.3V
2	I2C_SCL	1SPI_MOSI/5TX	+3.3V	GND
3	I2C_SDA	1SPI_MISO/5RX	CS0-	RST-
4	IRQ5B- / 4CTS	1SPI_SSN3-/4TX	CS1-	ADD0
5	IRQ4B- / 3CTS	1SPI_SSN2-/3TX	CS2-	ADD1
6	WAIT-	1SPI_SSN1-/4RTS	CS3-	ADD2
7	GND	1SPI_SSN0-/3RTS	CS4-	CLK0
8	ADD27	IRQ7B- / 4RX	DATA0	GND
9	ADD26	IRQ6B- / 3RX	DATA1	WRITE-
10	ADD25	DATA31 / IO7B	DATA2	ADD3
11	BE3-	DATA30 / IO6B	DATA3	ADD4
12	BE2-	DATA29 / IO5B	DATA4	ADD5
13	GND	DATA28 / IO4B	DATA5	READ-
14	BE1-	DATA27 / IO3B	DATA6	GND
15	BE0-	DATA26 / IO2B	DATA7	ADD6
16	ADD24	DATA25 / IO1B	DATA8 / IO0A	ADD7
17	ADD23	DATA24 / IO0B	DATA9 / IO1A	ADD8
18	OE-	DATA23	DATA10 / IO2A	ADD9
19	GND	DATA22	DATA11 / IO3A	ADD10
20		DATA21	DATA12 / IO4A	GND
21	ADD22	DATA20	DATA13 / IO5A	ADD11
22	ADD21	DATA19	DATA14 / IO6A	ADD12
23	ADD20	DATA18	DATA15 / IO7A	ADD13
24		DATA17	IRQ2A- / 0RX	ADD14 /WAIT-
25	GND	DATA16	IRQ3A- / 1RX	ADD15 /BE0-
26	CLK1 (S-CLK0)	CS9-	0SPI_SSN0-/0RTS	GND
27	ADD19	CS8-	0SPI_SSN1-/1RTS	ADD16 /BE1-
28	ADD18	CS7-	0SPI_SSN2-/0TX	IRQ0A- /0CTS
29	ADD17	CS6-	0SPI_SSN3-/1TX	IRQ1A- /1CTS
30	RST-	CS5-	0SPI_MISO/2RX	I2C_SDA
31	GND	+3.3V	0SPI_MOSI/2TX	I2C_SCL
32	+3.3V	VAUX0 / +12V	0SPI_CLK	GND

PIN	ROW A	ROW B	ROW G	ROW H
1	GND	1BPL_CLK	VAUX1 / +12V	+3.3V
2	I2C_SCL	1BPL_M0B1	+3.3V	GND
3	I2C_SDA	1BPL_M1B0	CS0-	RST#
4	IRQ5B- / 3RTS	3Rx / 1BPL_BSN2-	CS1-	ADD0
6	IRQ4B- / 3CTS	3Tx / 1BPL_BSN2-	CS2-	ADD1
8	SCLK4	2Rx / 1BPL_BSN1-	CS3-	ADD2
7	GND	2Tx / 1BPL_BSN0-	CS4-	CLK0
8	SCLK3	IRQ7B- / 2RTS	DATA0	GND
9	SIO17	IRQ6B- / 2CTS	DATA1	WRITE-
10	SIO16	SIO15 / IO7B	DATA2	ADD3
11	S-STAT5	SIO14 / IO6B	DATA3	ADD4
12	S-BYND0	SIO13 / IO5B	DATA4	ADD5
13	GND	SIO12 / IO4B	DATA5	READ-
14	SCLK2	SIO11 / IO3B	DATA6	GND
16	S-STAT6	SIO10 / IO2B	DATA7	ADD6
18	S-STAT7	SIO9 / IO1B	DATA8 / IO0A	ADD7
17	S-STAT6	SIO8 / IO0B	DATA9 / IO1A	ADD8
18	SCLK1	SIO7	DATA10 / IO2A	ADD9
19	GND	SIO6	DATA11 / IO3A	ADD10
20	S-READ0	SIO5	DATA12 / IO4A	GND
21	S-STAT5	SIO4	DATA13 / IO5A	ADD11
22	S-STAT4	SIO3	DATA14 / IO6A	ADD12
23	S-STAT3	SIO2	DATA15 / IO7A	ADD13
24	S-WRITE0	SIO1	IRQ2A- / 0CTS	ADD14 / WAIT-
26	GND	SIO0	IRQ3A- / 0RTS	ADD15 / BEC-
28	CLK1 (S-CLK0)	S-BEL4	0Tx / 0BPL_BSN0-	GND
27	S-STAT2	S-BEL3	0Rx / 0BPL_BSN1-	ADD16 / BE1-
28	S-STAT1	S-BEL2	1Tx / 0BPL_BSN2-	IRQ0A- / 1CTS
29	S-STAT0	S-BEL1	1Rx / 0BPL_BSN3-	IRQ1A- / 1RTS
30	RST#	S-BEL0	0BPL_M1B0	I2C_SDA
31	GND	+3.3V	0BPL_M0B1	I2C_SCL
32	+3.3V	VAUX1 / +12V	0BPL_CLK	GND

Power, ground, and major control pin locations are such that rotation of full and half cards by 180 degrees can be implemented (half cards at A1 or H32 orientation). Support for single side operation is also supported (for example, row GH or AB only for insertion into a vertical carrier card).

Row GH contains primary, 16 bit, asynchronous, memory mapped IO bus as well several serial interfaces.

Row AB is a functional duplicate of GH and adds serial ports, synchronous IO bus, and power/control pins to support a half card located in H32 orientation (half cards can be located at both ends, A1 or H32 orientation).

Discrete IO should be placed on IO0A-IO7A and IO0B-IO7B (secondary function). This results in 8 bit interfaces (instead of 16 bit).

Synchronous FIFO type interface. Signals are mapped similarly to row GH and can alternately be used as a second 16 bit asynchronous bus or expanded to provide a single 32 bit asynchronous bus.

Figure 9: Standard Card Pin Functional Grouping (128 pin)

PIN	ROW A	ROW B	ROW G	ROW H
1	GND	1BPL_CLK	VAUX1 / +12V	+3.3V
2	I2C_SCL	1BPL_M0B1	+3.3V	GND
3	I2C_SDA	1BPL_M1B0	CS0-	RST#
4	IRQ5B- / 3RTS	3Rx / 1BPL_BSN2-	CS1-	ADD0
6	IRQ4B- / 3CTS	3Tx / 1BPL_BSN2-	CS2-	ADD1
8	SCLK4	2Rx / 1BPL_BSN1-	CS3-	ADD2
7	GND	2Tx / 1BPL_BSN0-	CS4-	CLK0
8	SCLK3	IRQ7B- / 2RTS	DATA0	GND
9	SIO17	IRQ6B- / 2CTS	DATA1	WRITE-
10	SIO16	SIO15 / IO7B	DATA2	ADD3
11	S-STAT5	SIO14 / IO6B	DATA3	ADD4
12	S-BYND0	SIO13 / IO5B	DATA4	ADD5
13	GND	SIO12 / IO4B	DATA5	READ-
14	SCLK2	SIO11 / IO3B	DATA6	GND
16	S-STAT6	SIO10 / IO2B	DATA7	ADD6
18	S-STAT7	SIO9 / IO1B	DATA8 / IO0A	ADD7
17	S-STAT6	SIO8 / IO0B	DATA9 / IO1A	ADD8
18	SCLK1	SIO7	DATA10 / IO2A	ADD9
19	GND	SIO6	DATA11 / IO3A	ADD10
20	S-READ0	SIO5	DATA12 / IO4A	GND
21	S-STAT5	SIO4	DATA13 / IO5A	ADD11
22	S-STAT4	SIO3	DATA14 / IO6A	ADD12
23	S-STAT3	SIO2	DATA15 / IO7A	ADD13
24	S-WRITE0	SIO1	IRQ2A- / 0CTS	ADD14 / WAIT-
26	GND	SIO0	IRQ3A- / 0RTS	ADD15 / BEC-
28	CLK1 (S-CLK0)	S-BEL4	0Tx / 0BPL_BSN0-	GND
27	S-STAT2	S-BEL3	0Rx / 0BPL_BSN1-	ADD16 / BE1-
28	S-STAT1	S-BEL2	1Tx / 0BPL_BSN2-	IRQ0A- / 1CTS
29	S-STAT0	S-BEL1	1Rx / 0BPL_BSN3-	IRQ1A- / 1RTS
30	RST#	S-BEL0	0BPL_M1B0	I2C_SDA
31	GND	+3.3V	0BPL_M0B1	I2C_SCL
32	+3.3V	VAUX1 / +12V	0BPL_CLK	GND

Row GH provides power and access to 8 data bits of the asynchronous IO bus (for half cards).

Row AB provides access to the serial interfaces as well as IRQ signals. Synchronous bus pins (gray highlight) are not defined for half cards, and can be used for extra IO if the synchronous bus is not utilized.

Secondary half card location provides identical pin access if the half card is rotated by 180 degrees and inserted (H32 orientation). Rotation of half cards also provides for proper orientation of IO connectors on either end of full card (IO connectors point out from stack).

Figure 10: Half Card Pin Functional Grouping (inserted on 128 pin card)

9 Pin Function Definition

Tables of pin function definition for both the **standard pin headers** (rows A, B, G, H) and **expanded pin headers** (rows C, D, E, F) are available for download from www.cardstac.com. Pin function table files are available in .xls (spreadsheet) format.

10 Isolated Bus Grouping

Cardstac modules are primarily intended to be used in a parallel bus topology. Therefore, each pin number in a stack of cards or on a carrier is connected to every other pin number in parallel. For some design implementations, it might be necessary to have isolated bus groups. Isolated bus groups can be used to interface incompatible Cardstac bus implementations. Or, an example that requires isolated bus groups is the design case where a CPU processor card must be connected to prototype circuits through an FPGA interface. The CPU processor card nets and prototype circuit nets must not be on the same pins, but connected via an interfacing FPGA device. This application requires isolated bus grouping which is not possible on all pins when they are connected in parallel using a stack configuration.

On a carrier, isolated bus groups require a bridge or central control device (typically a higher IO count BGA FPGA). The 256 pin expanded card type can provide two completely isolated 110 pin signal groups when used on a carrier. Each bus group is located to either side of a centrally located 256 pin card. The pin-out of the expanded card allows complete bus isolation for two 128 pin cards located to each side. PCB pin placement is such that each signal type can flow directly from one side of the 256 pin bridge card, through a bridging device (FPGA), to the other side. Or, the FPGA device might contain a processor IP core that controls each individual bus group located to each side. This is a primary reason for utilization of a 256 pin expanded card (isolated bus control or bridge). A diagram of possible isolated bus topologies is shown on the next page.

Cardstac Isolated Bus Configurations

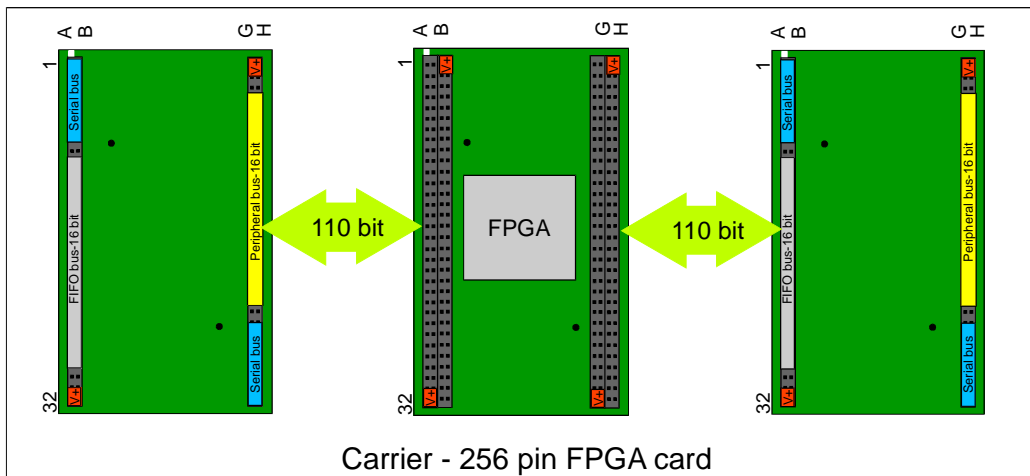
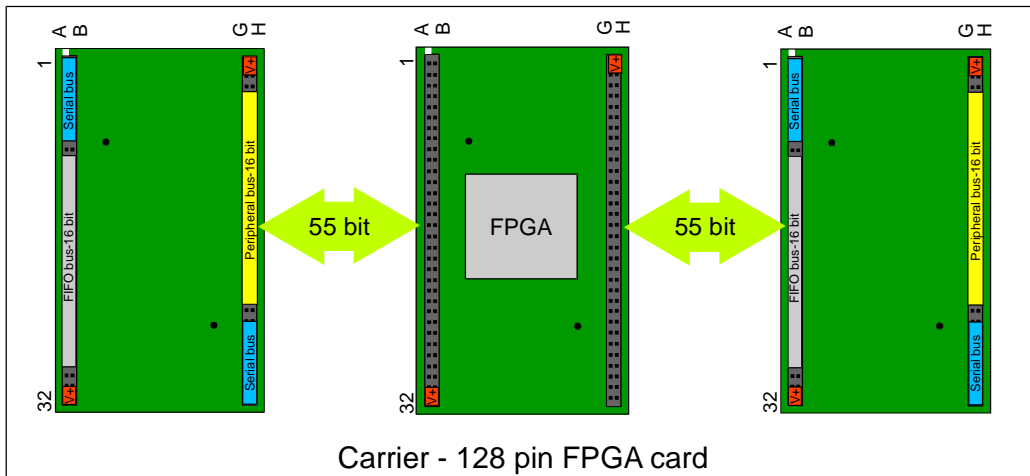
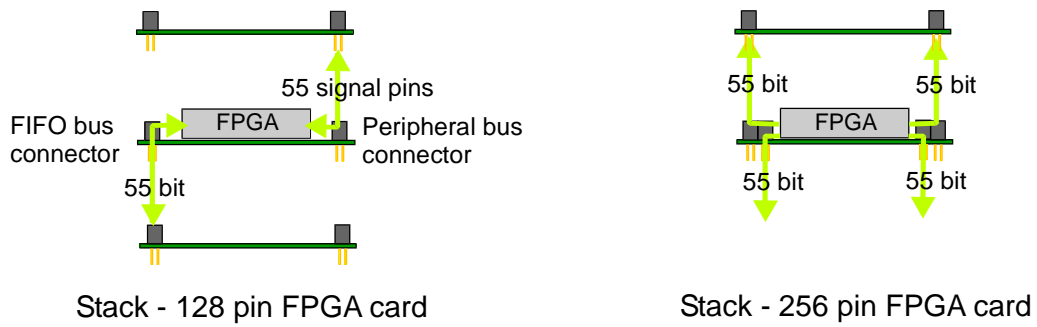


Figure 11: Cardstac Isolated Bus Configurations

11 Digital Pin Logic Level

Designers should always use 3.3V LVTTTL logic levels for Cardstac digital IO pins. Specific applications may require the use of other logic levels, but compatibility with most other Cardstac products will be eliminated.

12 Power

Power for a Cardstac system can be provided by a master card, slave card, or a dedicated power card. For modules that are mounted on a PCB carrier, power can also be provided by the PCB carrier. In instances where power is regulated locally on a module and then distributed to a stack using the module power pins, provisions should be made to allow disabling power output if necessary. This will allow use of these modules in systems where power is already provided by another means. Fusing should be provided on all power input nets for Cardstac modules. Power input pins should be combined to a common net on the PCB, and then subsequently pass through a fuse before entering a PCB power plane or distribution trace. **The power pins of a Cardstac system should be checked closely due to the configurable nature of power provisioning.**

Cardstac module power pins are physically located so that power can be supplied to two half cards located at each end of a host standard card. When cards are located in a stack, a **two Ampere per-pin current limit applies to the entire system** (stack). When modules are on a carrier, this limit applies to each stack located on the carrier (power distribution is done using carrier plane/trace copper). The Cardstac power specification is summarized in the table below:

Table 6: Power Specifications

Voltage	Standard Pin	Expanded Pin	Min./Max. Voltage (measured at load)	Max. Current
+3.3V	A32, B31, G2, H1	C2, D1, E32, F31	3.14 - 3.46V (3.3V +/-5%)	2 Ampere per pin
Vaux0 / +12V	B32, G1		11.4 – 12.6V (12V +/-5%) +30V DC maximum -30V DC minimum	2Ampere per pin
Vaux1		C1, F32	+30V DC maximum -30V DC minimum	2Ampere per pin

+/-30V DC voltage rating implies that general use products such as carrier cards should use components which will work with +/- 30V DC on the Vaux power rails. A proper voltage rating for all Vaux components is necessary, and components like polarized electrolytic capacitors must be avoided. Cardstac modules (not general use carriers) only need to support the actual power configurations required by the design (Vaux is defined and not variable on a module). Note that **high current applications should not**

use **Cardstac module pins** for power distribution. Noisy, high current power applications (motors, transistor drivers, lamps, etc) should distribute power using a separate wire harness and connector located on each module. Distributing high current power on the Cardstac module pins will result in high levels of ground noise riding on the digital signals (unless very good power filtering is used on each module).

The 3.3V power rail voltage should not be changed, and is provided for digital components in a Cardstac system. Local, on-card regulation is recommended for lower digital voltages. The Vaux pins are provided for system wide power distribution of a specific voltage level that will be required on multiple cards. For example, Vaux0 can be used to distribute a quiet “analog” 12V supply voltage to all cards in a stack. The Vaux0 and Vaux1 pins can be used for any voltage level up to 30V DC. If 12V is present in a system, this voltage level should be placed on Vaux0 (reserved location for +12V)

The Vaux power pins might be used to distribute core voltages for digital ICs such as FPGA devices (1.5V, 1.2V). Although convenient for use in a FPGA based Cardstac system, this will preclude the use of the FPGA card with another card type that uses the same Vaux pin (for example, Vaux0 with 12V). To provide maximum compatibility with other Cardstac modules, a better strategy would be to derive digital voltages from the 3.3V supply input using local regulation and leave the Vaux0 pin open. For specialized digital designs where compatibility is not important Vaux0 can be used for additional digital voltage rails.

A standard 128 pin card has two Vaux0 power pins (G1 and B32). It is possible to drive these two pins with two different voltage levels. This is not recommended, as standard cards must be inserted with A1 alignment only, and half cards will be limited to working on one end of standard card only (because Vaux0 pin provisioning is not symmetrical). Because of the “end to end symmetry” required for Cardstac power implementation, **do not drive Vaux0 or Vaux1 pin pairs with two separate voltages**. Always insure that the voltage on pin B32 = G1.

Expanded connectors C, D, E, and F also provide extra power and ground pins which are similar to the power and ground pin mapping on standard connector rows A, B, G, and H. Although expanded connector Vaux1 pins can provide a different voltage than Vaux0, both pins of Vaux1 should also be driven to the same voltage (C1 = F32).

Although the contact resistance of pin headers is relatively low (on the order of 10-20 milli-Ohms), for higher current applications, the voltage drop across header pins should be considered. Our tests have shown a 0.067V drop across a 5 card stack at 2A current. Pin headers are usually specified anywhere from 1A to 5A maximum per pin, so insure that you have an appropriate header for your application.

13 IO Connector Placement

The open ends of a Cardstac module are used for power input and IO connectors. The ends of the module are free of tooling holes to maximize available PCB area for connector placement. IO connectors should always be placed on the top PCB side only (0.080 inch height limit for bottom side components).

Notice the “end-tab” areas located on the Cardstac module shown in the diagram below. The end-tab areas are provided so that Cardstac modules can be (as an option) inserted into enclosures or inserted into vertical carriers using card guides (module using a right angle pin header).

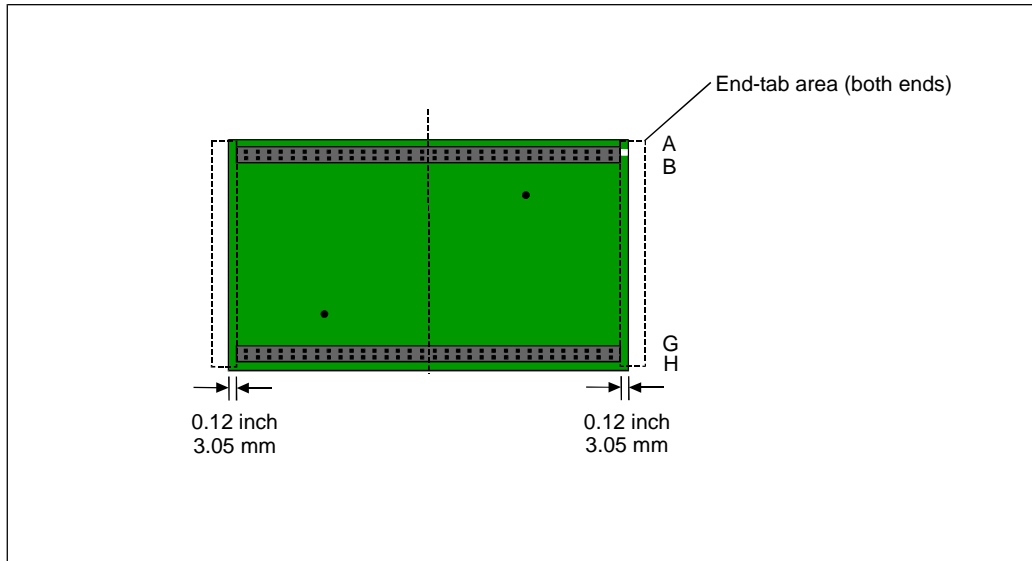


Figure 12: End Tab Areas

There are three possibilities for component and IO connector placement at the open ends of a Cardstac PCB.

- Components and connectors are placed so that they do not extend into the “end-tab” area.
- Components can be placed all the way to the end of the card, and IO connectors can be placed so that connector edges line up with the PCB edge.
- Components can be placed all the way to the end of the card, and IO connectors can be placed so that extension past the PCB edge is allowed (over-hang).

These three component placement techniques will affect how a specific design will interact with an enclosure or card guide. For maximum system flexibility, module components and connectors should not extend into the end-tab area. IO modules may require connector placement at, or over the edge of the PCB for proper enclosure alignment (in the end-tab area).

IO connector placement on half cards should be on the A1 end of the card only. This is so IO connectors will be positioned properly when a half card is placed at both ends of a host standard card. Figure 7 shows proper half card orientation and IO connector placement.

14 Airflow and Stack Cooling

IO connector placement at the ends of Cardstac modules restricts airflow, and therefore, cooling rates of electrical components located centrally to the module. This applies only to cards that will be located in the center of a stack (rather than on top). The long 128 or 60 pin headers (for module rows A, B, G, H)

already restrict airflow over module components. If other connectors on the end of cards completely obstruct the opening, the internal devices on the module will not be able to shed heat effectively.

High power devices should be restricted to operation on the top or bottom of a stack (or forced airflow through the stack should be implemented). High power devices that are low profile should not be placed on the bottom side of a Cardstac PCB. Bottom side clearance is very limited if a module is soldered directly into a carrier (0.1 inch or 2.54 mm). This tight, bottom side clearance will restrict airflow and heat removal from the high power device. Use of any type of stack enclosure also requires careful consideration of device power consumption and airflow. Simple enclosure slots might be adequate, but fans located on the enclosure may be required for adequate cooling of high power components. Fans (or primary air flow direction) should be oriented to move air through the open ends of a card stack.

It is possible to omit the 0.1 inch spacer located on the bottom side of Cardstac modules. This will leave a short length of bare pins exposed under each module after stack insertion (at the point of entry into the connector below). This will improve heat removal for components when the stack is in open-air conditions. When using forced-air cooling, maintaining a closed air channel through the stack may be preferable.

15 Stacking Limits

As cards are added to a stack, loading on each pin goes up as well as power requirements for the stack. As the +3.3V power bus contains four pins (using standard 128 pin-out), there is a limit on the amount of power that can be distributed using the dedicated header pins (two Ampere per pin).

A practical limit to a stack is five cards. Many more could be added if card power consumption is low or an alternative power distribution method is used. Edge rate and operating frequency of data signals would also have to be low.

The standard 128 pin signal definition supports five chip select signals (CS0- thru CS4-). This implies a logical limit of one master card and five slave cards for a total of six cards (assuming one chip selected entity per card).

16 Signal Integrity and Signal Termination

PCB trace impedance of digital nets on Cardstac modules should be designed to provide an impedance of **50 ohms**. This is achieved by adjusting the trace geometry with respect to a reference plane (typically a ground plane). Both master and slave cards should provide signal termination if required. Carrier cards can also provide termination, although carrier designs are typically general purpose in nature and are not ideal for implementing specific termination strategies. Pull-up resistors should be located on master cards only. Signal integrity and termination are not covered in detail by this specification. Some basic guidelines include:

- Signals which are very high speed and sensitive to edge smoothness should use a low skew, controlled impedance connector designed for the specific application (not pin headers).

- There will be an increase of net impedance (impedance discontinuity) for signals that travel over the module pin headers. This is acceptable for digital signals that have a reasonable edge rate, net loading, and minimal overall trace length.
- Use of contiguous (no large slots or cut-outs) ground plane greatly improves signal integrity and reduces radiated EMI and noise (from PCB). Always provide a ground plane on modules and carrier cards. Cardstac pin mapping provides multiple ground return pins along the entire length of the main header connectors.
- Termination can be provided for clock and control signals (edge control such as a write signal). Signal termination is not as important for “data” signals, which are qualified by clock or control signal edges.
- Source series termination is simple and typically provides good results, especially for nets that are single source. Signal integrity will be the best towards the far end of the trace (star or daisy chain topology). Use a series terminator value that matches the output impedance of the driver to the PCB trace impedance (generally 33 ohms).
- Bi-directional nets can use source series termination at each driver, or perhaps termination at each end of the physical bus.
- Signal integrity on digital signals is primarily related to transition edge speed and smoothness of the edge, rather than operating frequency. Low frequency control signals still require termination if the transitioning edge rate is high. Termination is important once a net becomes long and is not a “lumped element” (exhibits transmission line characteristics).
- Most FPGA and EPLD devices can provide programmable termination on each pin.

17 Electrical Performance

Cardstac is intended as an “inter-connect” specification. Operational performance of Cardstac circuits will depend on many parameters of a design implementation (number of cards in stack, pin loading, stub length on module PCB, circuit type, etc.) The peripheral and FIFO bus signals are defined and mapped to the header connectors in a recommended. The clock and control signals are positioned adjacent to ground pins to provide optimal signal integrity.

Some benchmark performance numbers are provided in the following table. These numbers are listed as an example of the bus performance that can be provided by a typical Cardstac system operating at room temperature and nominal voltage. The system was implemented with Altera Cyclone II FPGA devices with on-chip series termination enabled. The system was comprised of one master card and up to five slave cards. FIFO bus write and read loop-back tests (16 bit) were performed to and from each slave card at various operating frequencies. The system was finally pushed to the point of failure. The results are as follows:

Table 7: Cardstac FIFO Bus Performance Example

Module Connector Pin Operating Speed	3 Card Stack	5 Card Stack	6 Card Stack	Test Duration
10 Mhz	tbd	tbd	tbd	30 minutes
25 Mhz	tbd	tbd	tbd	30 minutes
50 Mhz	tbd	tbd	tbd	30 minutes
75 Mhz	tbd	tbd	tbd	30 minutes
100 Mhz	tbd	tbd	tbd	
125 Mhz	tbd	tbd	tbd	
150 Mhz	tbd	tbd	tbd	

Note that the failure point is caused by bus timing violations. Methods for adjusting the timing (clock or signal skew) were not implemented to improve performance. The results confirm that bus operating frequencies of 10 MHz to 50 MHz are a possible working range for Cardstac systems. Faster bus speeds can be achieved, but will require attention to implementation details.

18 Mechanical Dimensions

Mechanical dimensions for card vertical spacing and board outline must be fixed to maintain Cardstac interoperability. The diagram below shows the vertical spacing for Cardstac modules. By using a 0.1 inch thick bottom side plastic spacer (press fit over pin-tails protruding from the bottom of the PCB), 0.435 inch clearance can be maintained for all types of connectors in a stack. Each module in a stack uses 0.497 (12.6 mm) of vertical space when the thickness of the PCB is included in the total.

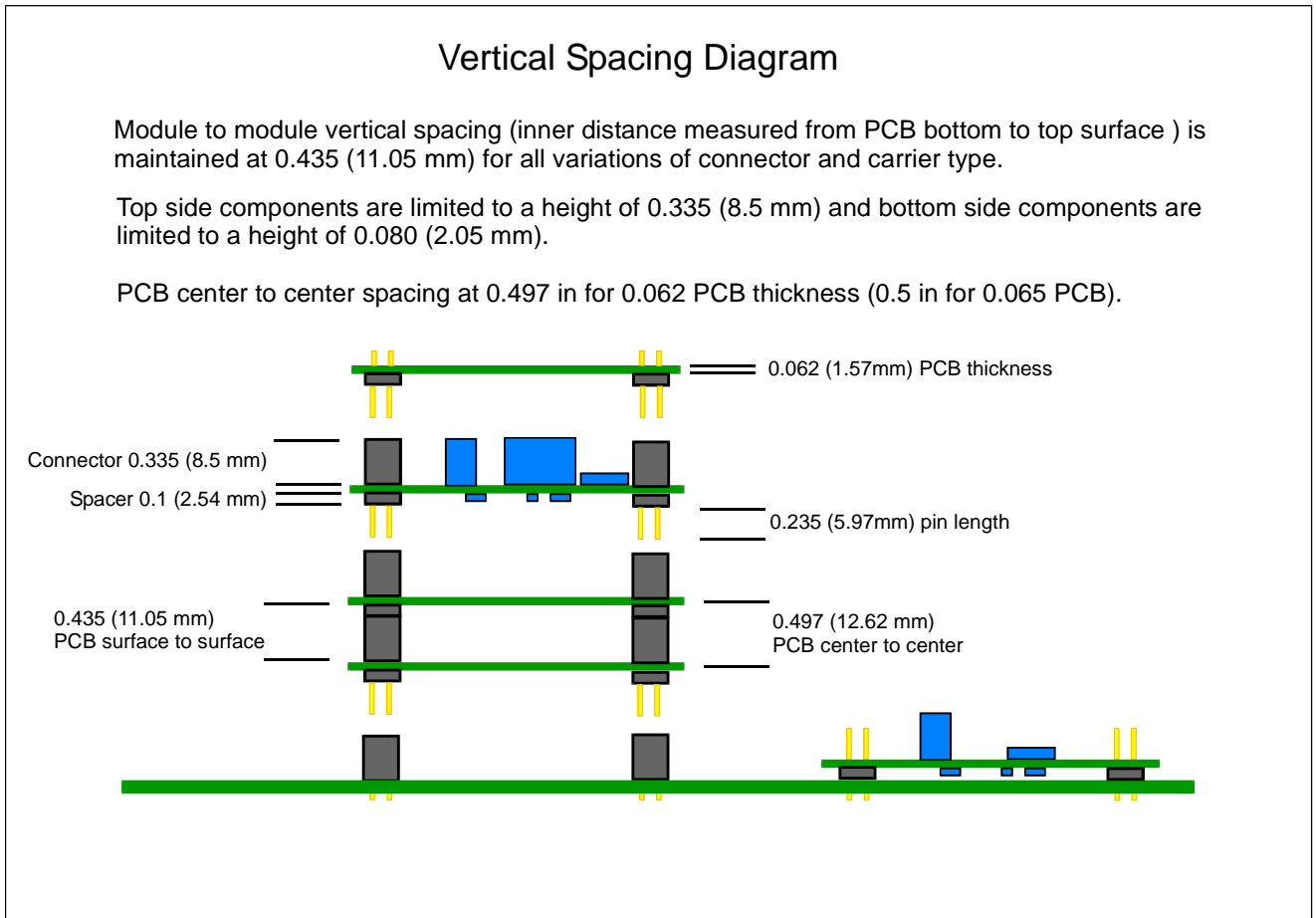


Figure 13: Cardstac Module Vertical Spacing

The mechanical requirements for Cardstac modules/components are summarized below:

1. **PCB Thickness:** should be 0.062 inch +/- 0.005.
2. **Module Connectors:** are based on 0.1 inch pitch pin headers containing 64 (standard card) and 30 (half card) pin counts. If stacking capability is desired, then a “stack-thru” type female header must be utilized. An overall connector height of 0.435 inch (11.05 mm) is required to maintain proper board to board spacing. For a 0.335 (8.5 mm) high connector, a 0.1 (2.54 mm) spacer must

be added. Connectors are also available that are 0.435 (11.05 mm). Available pin-tail length for insertion into a connector should be 0.235 (6.0 mm). Therefore, with a PCB thickness of 0.062, overall connector pin-tail length should be 0.395 (10.0 mm). Longer pin-tail lengths can be used in conjunction with more spacers to increase board to board spacing

3. **Stand-offs:** are necessary if a secure and vibration resistant method of connecting modules within a stack is required. It is important that the overall stand-off height be slightly greater than the connector/spacer height. This is so the PCB will not be stressed (warped) when screwing the stand-offs together. A stand-off length of 3/8 (0.375) inch can be utilized in aluminum or nylon (with two washers for additional height). These stand-offs typically have a diameter of 3/16 (0.1875) inch. The stand-off thread should accept a 2-56 size screw.
4. **Screws:** size 2-56 (diameter of 0.085 inch). PCB mounting holes are 0.10 inch diameter.
5. **Washers:** diameter 3/16 (0.1875) and require a minimum thickness of 0.030 inch. Two washers are used (one at each end of stand-off) to provide 0.435 inch board to board spacing.
6. **PCB Keep-out Area:** should be round with a diameter of 0.220 inch centered at both mounting hole location (top and bottom side of PCB).
7. **Component Height, PCB Bottom:** Place only low profile components on the PCB bottom-side such as passive chip devices, or active devices that are in an IC package such as TSOP. Do not place components that exceed 0.080 inch (2.05 mm) height on the bottom side of the PCB.
8. **Component Height, PCB Top:** Module components located on the top-side of a PCB are limited to a height of 0.335 inch (8.5 mm). Modules that are only located on the top of a stack do not have this restriction (except as limited by enclosure dimensions).
9. **Connector Spacers:** are made of plastic and are used to set module to module spacing. Pin spacers are available in 0.10 inch (2.54 mm) thickness. Bottom side spacers press fit over the connector pin-tails. One spacer is used to provide 0.435 (11.05 mm) PCB surface to surface spacing. Use of additional connector spacers will require an equivalent increase in the stand-off height, and connector pin-tail length. Note that the spacers can be omitted.

The drawings shown on the following pages show dimensions for standard and half cards as well as stand-offs.

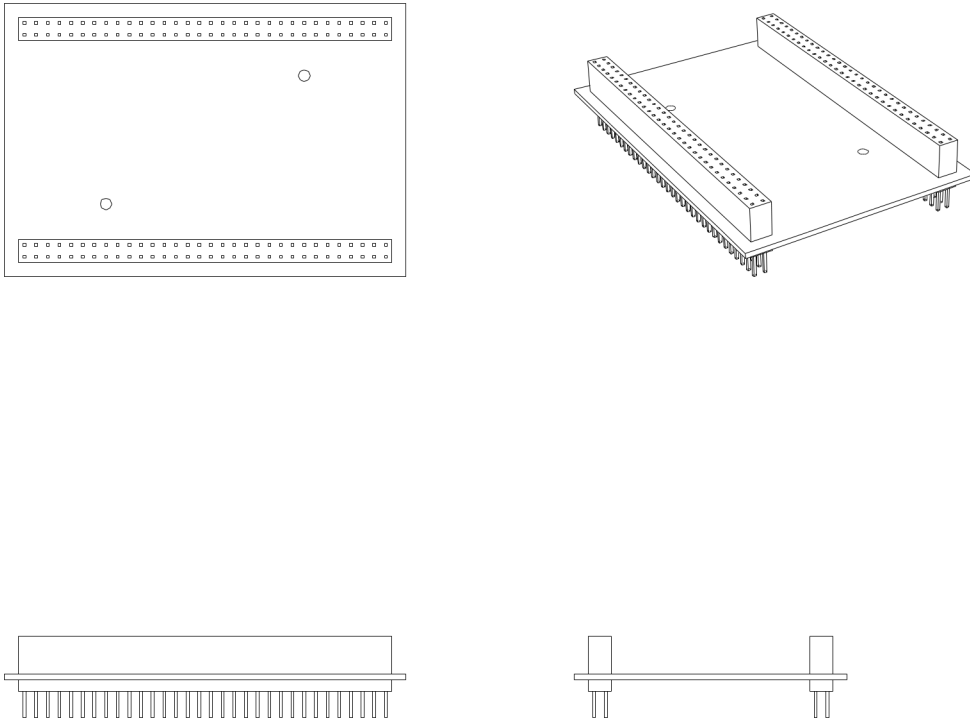


Figure 14: Standard Card Four Way View

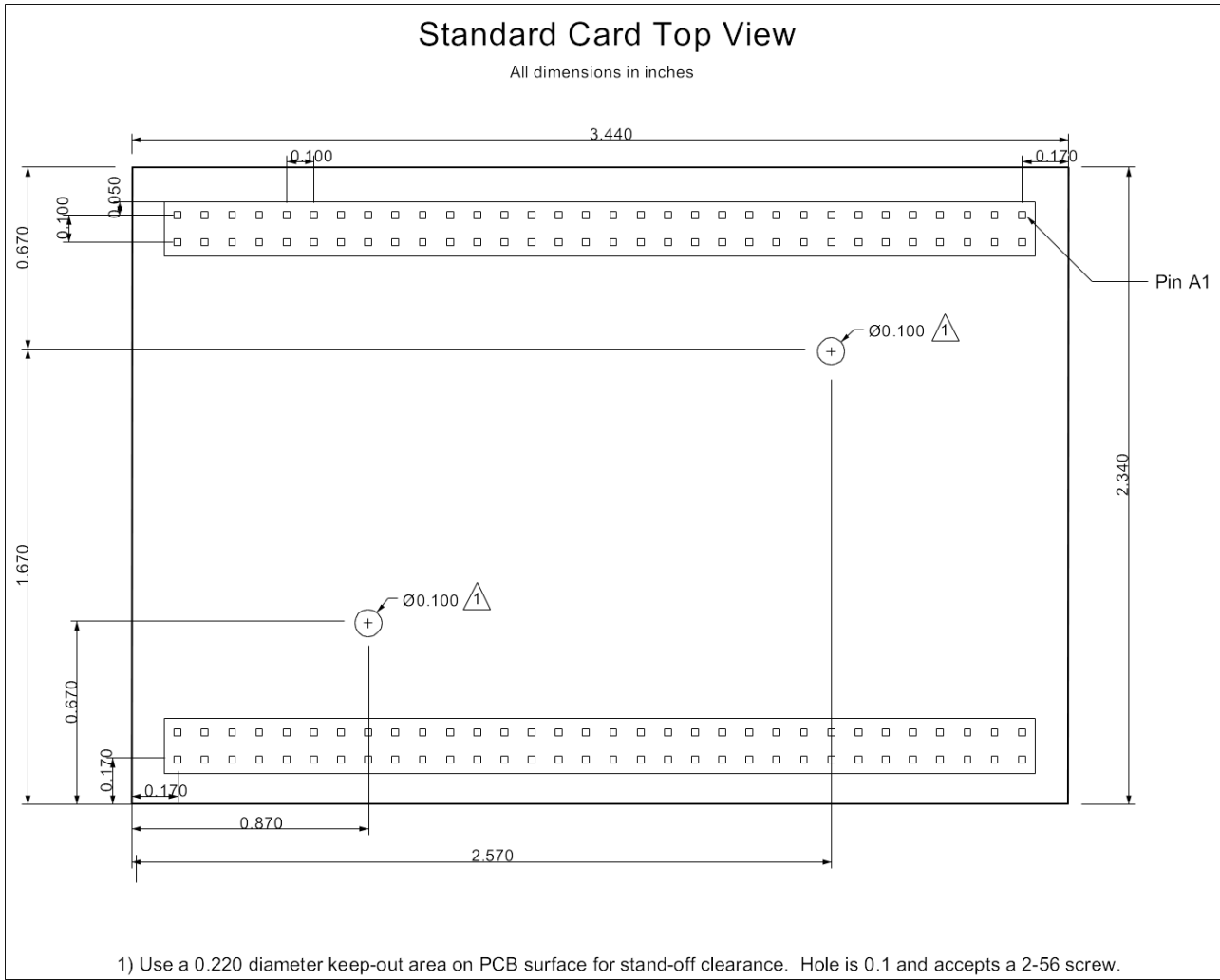


Figure 15: Standard Card Top View

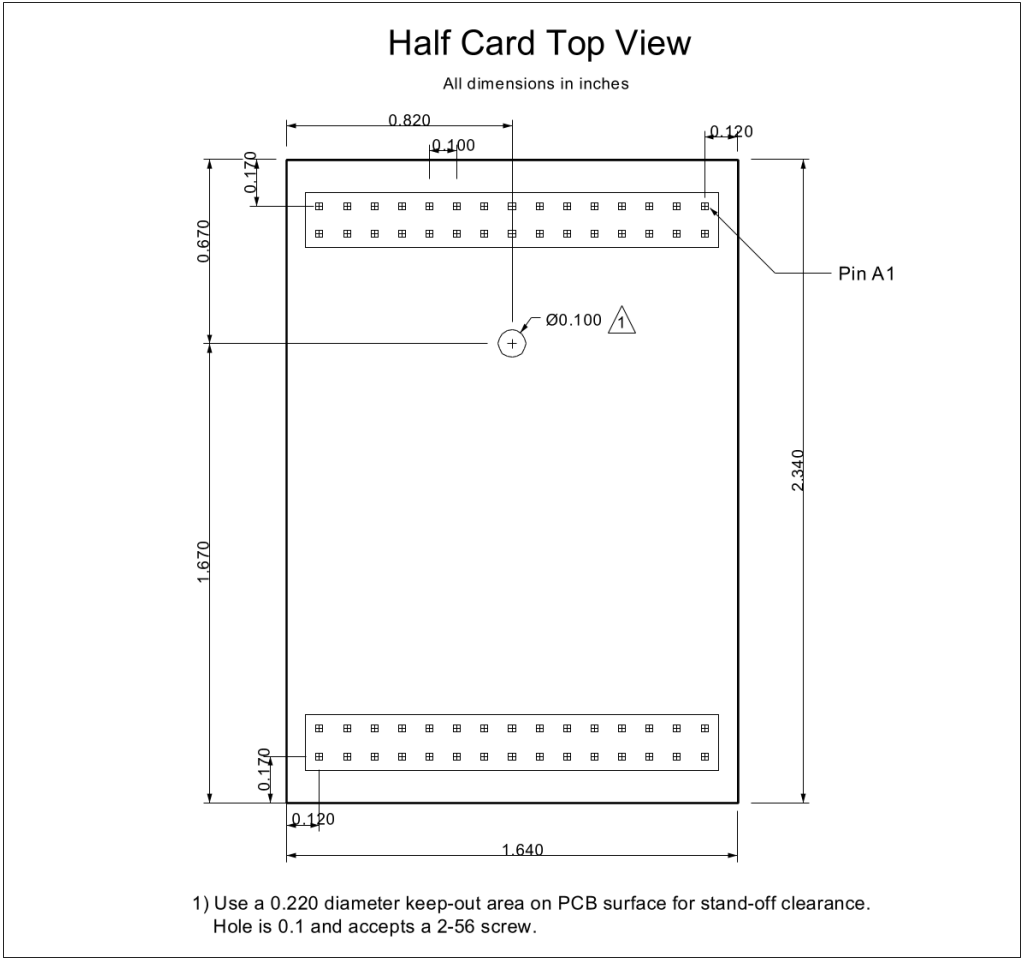
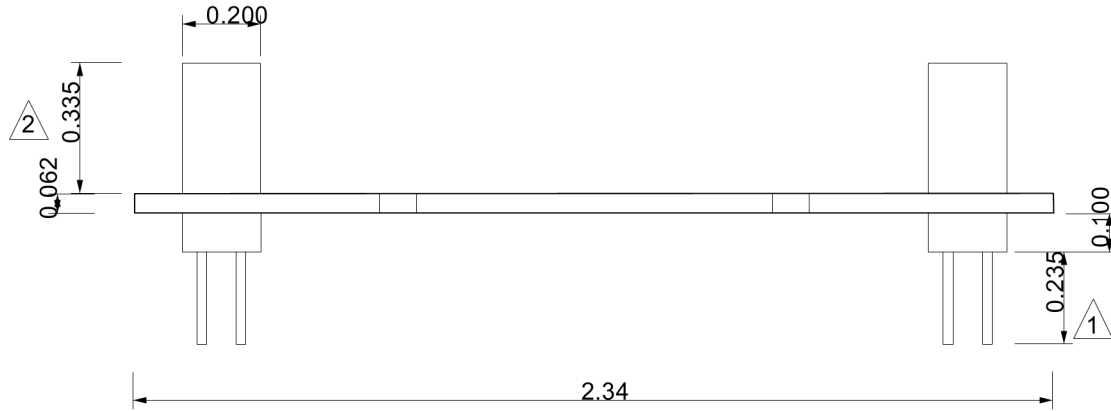


Figure 16: Half Card Top View

Standard and Half Card End View

All dimensions in inches



- 1) 0.235 typical. Pin tail length must be sufficient to allow proper mating with socket.
Typical mating pin length requirement for socket: 0.110 - 0.245.
- 2) Connectors at 0.435 height are also available.

Figure 17: Standard and Half Card End View

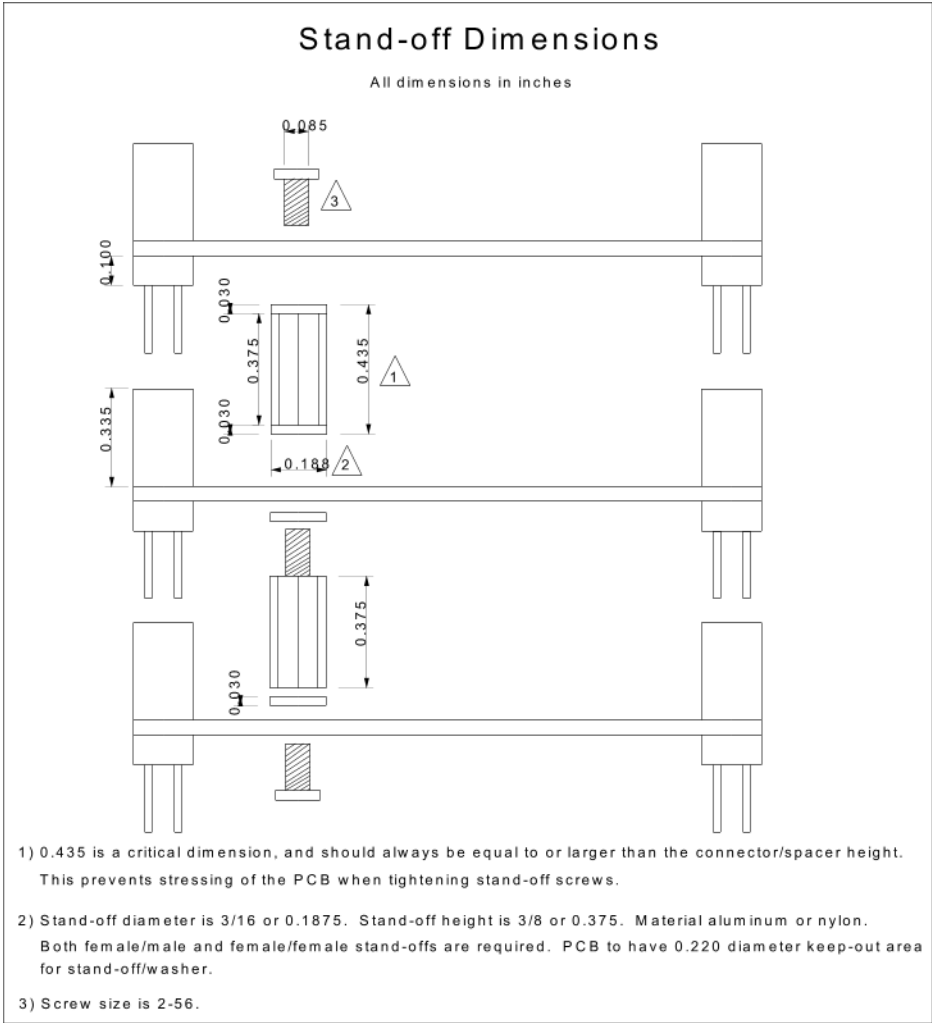


Figure 18: Stand-off Dimensions

19 Appendices

19.1 Appendix A - Cardstac Design for Compatibility

When mapping signals to Cardstac header pins, proper selection and configuration of control/interface signal nets will affect compatibility of the module with other Cardstac products. Some general guidelines to follow for a general use card are:

- Serial interface cards should support multiple interface standards when possible (I2C, SPI, serial Rx/Tx).
- General purpose IO lines are provided as a secondary function on the upper 8 bits of the Cardstac peripheral bus (D8 – D15). Cards that are designed for 16 bit peripheral bus operation, should also support 8 bit operation when possible. This will maintain compatibility with other cards that are using some of the upper data bits as general purpose IO.
- Configurable jumpers or resistors should be used to allow custom selection of a slave cards control/clock nets. For example, a SPI interface card should allow jumper selection of SSN0-, SSN1-, SSN2-, or SSN3- control. A synchronous digital interface card should ideally allow selection of clock input/output on any of the five available S-CLKIN pins (SCLKIN0-SCLKIN4) and circuit selection on any of the S-SEL pins (S-SEL0 – S-SEL4).
- Small EPLD devices can be utilized to allow programmable selection of pin mapping.
- On a particular Cardstac design, an EPLD device can be used to provide custom interfacing to local IC devices, and then provide a standardized “memory map” type interface on the Cardstac IO bus.
- An example processor card design might implement a memory mapped IO bus on rows G, H and analog to digital converter input pins on rows A, B. Although this is a valid design, the utilization of rows A, B for analog inputs will probably preclude the use of this processor card with another Cardstac product. A more compatible “overall” design would be to implement the analog input circuits on a separate dedicated A/D card. The digital results provided by the A/D circuits could be accessed via the standard Cardstac processor IO bus (row G, H).
- Open collector signal pull-up resistors should be located on master cards (rather than slave cards).

19.2 Appendix B – Stack-through Connectors and Solder

Stack-through pin headers provide Cardstac inter-connect. These pin headers are installed from the top side of the PCB with the pin tails protruding out the bottom side. A bottom side spacer can optionally be slid over the pin tails. Because of the pin-tails protruding through the bottom side of the PCB, these connectors must be given special care during the PCB assembly process. If solder residue is allowed to contact the pin-tails, these pins might not mate properly with another Cardstac module connector, and reliability will be compromised. Most of the assembly techniques for stack-through connectors were developed for PC/104™ products. The two types of assembly process that can be used to install the connectors are press-fit and solder.

1. **Press-fit:** these connectors remove the solder process completely. Press-fit connectors require a mechanical fixture for assembly, and also must not be used on thin PCBs. These connectors are typically more expensive than the equivalent solder on type. Press-fit connectors are not as common, and are usually available in 11mm or greater heights only (for PC/104™ form factor). The press-fit mechanism is a “needle eye” at the base of the pin. These connectors must be installed into a properly sized PCB hole, and can also present reliability issues when mechanical stress is applied to the connector.
2. **Solder:** these connectors are less expensive and more readily available. They can be found in both 11mm and 8.5mm heights. If hand soldered, installation must be completed by skilled assembly technicians, and solder residue on the pin-tails must be avoided. There are also some techniques that aid in the solder assembly process. These include:
 - Solder-forms, which are tiny solder rings. Solder forms are slipped over the pins of the connector, and then the connector is inserted into the PCB. The solder is melted during the PCB oven re-flow process.
 - Localized hot air re-flow can be provided by specialized production equipment, or manually with a SMT hot air rework gun. This process can be combined with solder forms, or after solder paste has been injected into the pin-tail hole on the PCB using a syringe.
 - Through Hole Reflow (THR) is a technique where through hole pads are stenciled (filled) with solder paste, and then the connector is pushed through the wet solder paste. The connector solder paste is then reflowed with the rest of the SMT components. This is a relatively new process (as of the time of this writing).

20 Disclaimer

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